CVC
Circuit Validity Checker

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CVC: Circuit Validity Checker

- What is it?
  - A system to pinpoint reliability errors that can lead to device failures or unintended current leakage.
  - Similar to Synopsys' CCK, Mentor's Calibre PERC, InsightEDA's Analyzer, or ICEE Solutions' Cratus.

- Background:
  - 22 years of backend verification experience with DRAMs, FLASH, and SOC's at Hitachi.
  - Includes 12 years developing CVC's proprietary predecessor which was used on over 400 tapeouts.
  - After Hitachi, developed a completely new system as open source.
  - Over 50 tapeouts. 16Gb DRAM, 3B transistor SOC's, etc.
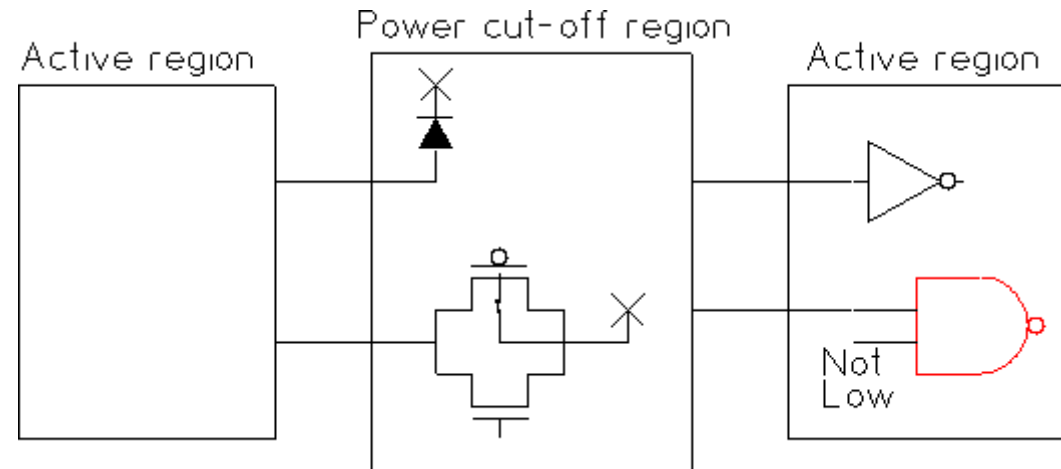
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- ## Error Types

  Gate vs source
  Forward bias diode
  Source vs bulk
  Fixed output
  Logically floating inputs
  Electrical overstress
  Leaks
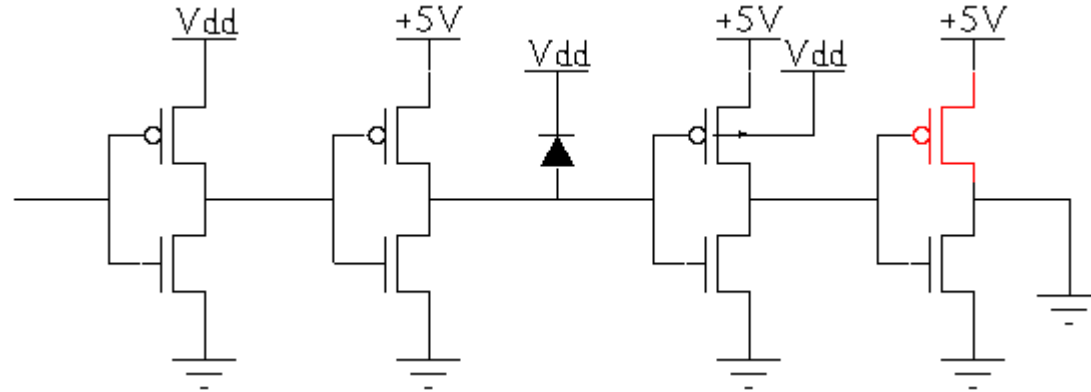
- ## Power cut-off errors

  Input to cutoff diodes
  Input to cutoff transfer gates
  Output to non-switched logic

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- Input is CDL used for chip level LVS
- Handles n/p-mosfets(enhancement & depletion), pnp/npn, diodes, and 2 & 3 terminal resistors and capacitors
- Redefine devices as on/off switches or fuses/anti-fuses
- Power and model parameters defined in MS-Excel
- Detects all error types on every run
- No rule files are needed
- Limit number of errors extracted per subcircuit
- Find all errors and categorize later. No waive file.
- Top-down or bottom-up analysis

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- Written in C++ for speed. Netlist input (bison/flex) is as fast as commercial programs (Calibre, Spicevision).
- Uses a fixed size three-dimensional dual b-tree event queue to prevent telescoping.
- Text uniquely stored in an obstack and referenced by address to speed comparison.
- Three types of signal propagation: minimum, logic, maximum.
- Change switches in model file to verify different configurations without changing the netlist.
- Set individual fuses as open or closed without changing the netlist.

For more information see
https://shuharisystem.com/logical/cvc/

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