Xyce: Open Source Simulation for Large-Scale Circuits

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ABSTRACT

This paper provides an overview of the open source analog simulation tool, Xyce, which was designed from the ground-up to perform large-scale circuit analysis. Current capabilities of the simulation tool will be discussed, including the analysis methods, device models, and parallel implementation. Future directions for expanding Xyce's capabilities and improving performance will be presented.

CCS CONCEPTS

• **Computing methodologies** → **Massively parallel and high-performance simulations**; *Parallel algorithms*; *Distributed simulation*; • **Applied computing** → **Computer-aided design**; *Physical sciences and engineering*;

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1 INTRODUCTION

The main purpose of circuit simulation is to aid in the design and verification of electrical and electronic circuits and systems prior to manufacturing and deployment. Analog circuit simulation is one of a hierarchy of approaches (Figure 1) that go from high-fidelity device (TCAD) simulations up to the digital level (gate level) and beyond (register transfer level, etc.). Mixed-signal simulation can greatly reduce the analog simulation time by replacing analog models with event-driven models for digital devices. Conversely, mixed-mode simulation adds fidelity by replacing analog models with PDE-based devices.

Current process nodes are pushing the development of simulation tools that can efficiently and effectively navigate the hierarchy of approaches, while scaling the circuit to unprecedented sizes. One such driver is the trend towards digitally-assisted analog/RF, and the development of Systems On a Chip (SOCs). Another driver is the challenge of design, verification, and debugging of mixed-signal systems, which is due to the presence of "analog issues," such as variability, noise/interference, nonlinear analog dynamics, analog waveshapes, and timing/phase lags. Often, for simulation of mixed-signal systems, simulation of the analog portions of the system are a significant bottleneck that cannot be avoided, as verification methods often require analog simulation results as an input.

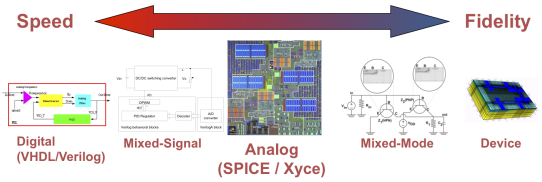

Figure 1: Hierarchy of Circuit Simulation Approaches

2 SPICE-STYLE ANALOG/RF SIMULATION

Time-domain (transient) and frequency-domain (HB) analog circuit simulations are an essential, yet expensive, part of the computer-aided design (CAD) process. This is because traditional analog circuit simulators, such as SPICE [5], are based on solving a fully-coupled nonlinear differential algebraic equation (DAE)

$$f(x(t)) + \frac{dq(x(t))}{dt} = b(t). \quad (1)$$

The traditional solution approaches do not scale well beyond tens of thousands of unknowns due to a reliance on a large single matrix that is usually treated by direct matrix solvers. As a result, the analog runtime scales super-linearly with increasing circuit size. For RF simulation, the scalability can be even worse than for transient, because harmonic balance (HB) analysis generates larger matrices that lack sparsity for the nonlinear portions of the problem.

SPICE-accurate simulation is often a prohibitive bottleneck in circuit design and verification. The speed penalty is can be mitigated by simulating only individual modules. Alternatively, it is natural to consider techniques that accelerate the analog simulation by using numerical approximations at various levels throughout the simulator. "Fast-SPICE" simulators rely on circuit-level, hierarchical partitioning algorithms, event-driven simulation techniques, and efficient surrogate models for devices and/or sub-circuits to perform faster, large-scale circuit simulations. While effective in many cases, the numerical approximations inherent to such algorithms can break down for modern feature sizes, especially in post-layout simulations where parasitics play a large role.

3 THE XYCE PARALLEL SIMULATOR

Xyce is a SPICE-compatible analog simulation tool [3], which has been under development since 1999. It has been designed to use distributed memory parallelism to address the scalability issues inherent to solving large nonlinear DAEs (1). From the beginning, the focus of Xyce development has been to provide scalable, numerically accurate analog simulation for large-scale circuits through

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the development and improvement of the algorithms at the core of SPICE-style simulation. Furthermore, Xyce has been designed to have a modular framework for integrating device models and developing state-of-the-art continuation algorithms, analysis methods, preconditioned linear solvers, and parallel partitioning techniques. In this section, we will take a look at several essential components of Xyce and discuss how they support the simulation of large-scale circuits for modern process nodes.

3.1 Device Model Support

Xyce includes legacy SPICE models, industry standard models (BSIM, PSP, MEXTRAM, VBIC, e.g.), and non-traditional models, such as memristors. The extensible design of the device model package, which defines the interaction between the analysis methods and the device models, has also enabled Xyce to be used for biological/reaction/neural network simulation and power grid simulation. For the integration of new compact models, Xyce also has a backend to the ADMS compiler, which translates Verilog-A to compilable Xyce C++ code. The C++ code can be compiled directly into Xyce's device model package, or dynamically linked to an existing Xyce binary. Alternatively, the Model and Algorithm Prototyping Platform (MAPP) [8], developed at Berkeley, provides translation from devices written in ModSpec [1], or the compilation of Verilog-A code via VAPP (the Verilog-A Parser and Processor). The resulting C++ device model can be passed into Xyce, using dynamic loading, through an API.

3.2 Analysis Capabilities

Xyce was initially developed to perform transient and DC analysis of analog circuits. The analysis capabilities have been extended to include AC, single-tone and multi-tone harmonic balance (HB), multi-time PDE (MPDE), model order reduction (MOR), direct and adjoint sensitivity analysis, and uncertainty quantification (UQ). Many of the newer analysis capabilities are also active areas of research, so the capabilities are improving with each release. Even the time-integration methods, which are key to the performance and accuracy of transient analysis, are constantly being improved with the addition of new Local Truncation Error (LTE) criteria.

3.3 Scalable Simulation

Achieving scalable parallel circuit simulation often comes down to striking the right balance of device distribution and the right choice of a linear solver. Since the inception of Xyce, the simulator has been designed to use a separate partition for devices and the linear solver. That is because the cost of evaluating a device model can vary greatly between device types and balancing that cost across processors can result in a matrix that is more challenging for linear solvers. Furthermore, as the scale of circuits increase—and assuming a reasonable distribution of devices—the dominant cost in the analysis quickly becomes the linear solver. To address this performance bottleneck, new parallel linear solvers and preconditioners [2, 6, 7] have been developed that enable the scalable transient simulation of postlayout ASICs with millions of devices.

An efficient, scalable linear solver is even more crucial for frequency-domain simulation than it is for transient simulation. Due to the fact that most device models can only be evaluated in the time domain, it is necessary to use Fourier expansions on the input and output variables of (1). After substitution and truncation (to M harmonics), the frequency-domain system is

$$H_{HB} = \Omega Q(X) + F(X) - B = 0, \tag{2}$$

where

$$\Omega = \begin{bmatrix} -Mj\omega_0 & & \\ & \ddots & \\ & & Mj\omega_0 \end{bmatrix}, \omega_0 = \frac{2\pi}{T}.$$

Compared to the linear system, of dimension n, generated by transient analysis, HB analysis will generate a linear system of dimension $n(2M+1)$ that is block structured, complex-valued, and possibly dense. Forming the matrix for HB analysis is not desirable, due to its size and structure, so iterative linear solvers are more appealing. Xyce provides efficient preconditioners and even a block direct linear solver that leverages sparsity from linear devices [4].

3.4 Future Directions

While Xyce is a highly-capable analog circuit simulator, many opportunities for improvements exist. Near-term efforts are focused on developing a mixed-signal API based on the Verilog Programming Interface (VPI). Future enhancements will revolve around creating better compatibility with industry standard simulators, such as HSPICE and Spectre. Areas of focus for these enhancements include both feature compatibilities and netlist parsing compatibilities. Finally, we are continuously improving Xyce's compact model support, whether it be via improvements in model speed, or by enhancing the feature support of the Verilog-A import capability.

Integrated circuits are often structured and hierarchical in nature, since many of the functional blocks within the circuit are developed independently. During the processing and setup of integrated circuits, this hierarchy is not preserved and the circuit is essentially "flattened." While Xyce has achieved success with this approach, hierarchical information will be leveraged in the future to develop better device distributions, linear solvers, and integrate "Fast-SPICE" techniques.

4 LICENSING AND AVAILABILITY

Xyce is open source software, released under the GNU General Public License, Version 3.0, since the release of Xyce 6.0 in 2013. Version 6.10 of Xyce is scheduled for release in October 2018. More information about the Xyce project, including software downloads and documentation, can be found on the website: https://xyce.sandia.gov.

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REFERENCES

[1] D. Amsallem and J. Roychowdhury. 2011. ModSpec: An open, flexible specification framework for multi-domain device modelling. In *2011 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*. 367–374.

[2] J. Booth, S. Rajamanickam, and H. Thornquist. 2016. Basker: A Threaded Sparse LU Factorization Utilizing Hierarchical Parallelism and Data Layouts. In *Proceedings of the 2016 IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW)*. ACM, 673–682.

[3] Eric R. Keiter, Heidi K. Thornquist, Robert J. Hoekstra, Thomas V. Russo, Richard L. Schiek, and Eric L. Rankin. 2011. Parallel Transistor-Level Circuit Simulation. In *Advanced Simulation and Verification of Electronic and Biological Systems*, Peng Li, Luís Miguel Silveira, and Peter Feldmann (Eds.). Springer, Chapter 1, 1–21.

[4] Amit Mehrotra and Abhishek Somani. 2009. A Robust and Efficient Harmonic Balance (HB) using Direct Solution of HB Jacobian. In *Proceedings of the 1009 Design Automation Conference*. ACM, 370–375.

[5] L. W. Nagel. 1975. *SPICE 2, a Computer Program to Simulate Semiconductor Circuits*. Technical Report Memorandum ERL-M250.

[6] Heidi K. Thornquist, Eric R. Keiter, Robert J. Hoekstra, David M. Day, and Erik G. Boman. 2009. A parallel preconditioning strategy for efficient transistor-level circuit simulation. In *2009 IEEE/ACM International Conference on Computer-Aided Design - Digest of Technical Papers*. 410–417.

[7] Heidi K. Thornquist and Siva Rajamanickam. 2014. A Hybrid Approach for Parallel Transistor-Level Full Chip Circuit Simulation. In *High Performance Computing for Computational Science - VECPAR 2014*, M. Dayde, O. Marques, and K. Nakajima (Eds.). Springer.

[8] T. Wang, K. Aadithya, B. Wu, and J. Roychowdhury. 2015. MAPP: A platform for prototyping algorithms and models quickly and easily. In *2015 IEEE MTT-S International Conference on Numerical Electromagnetic and Multiphysics Modeling and Optimization (NEMO)*. 1–3.