Towards an Open-Source Verification Method with Chisel and Scala

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State of the Art

- Most HW designs are in VHDL or Verilog
  - Quite old languages
- Modern concepts such as OO and FP missing
- SystemVerilog adds OO for verification
  - Code coverage and constraint random generators
  - Now 250 keywords in the language
  - OO not usable for design description
- Universal Verification Method (UVM)

UVM

- Open-source SystemVerilog classes
  - Is an industry standard
  - Adaption?
- A blueprint to define tests
  - Make tests reusable
- Main approach to compare against a reference model
- Use SV constraint random test vector generation
- Use SV coverage metrics

Chisel and ChiselTest

- Chisel is a new hardware construction language
- Embedded in Scala, which runs on a JVM
- Many Scala and Java libraries are available
- Generates Verilog for synthesis
- OO and FP usable for hardware description
- ChiselTest is a testing framework for Chisel
  - Basic setting of inputs and reading outputs of a DUT

What is Missing?

- A UVM ‘like’ verification framework
- Mixed language support (VHDL)
- Constraint random generation
- Coverage measurements
- Library of test components
  - E.g., bus functional models

First Experiments

- Using Chisel and UVM on a small test circuit
- An ALU with an accumulator
- Written in Chisel and in VHDL
- Tested with Chisel and UVM
- Using Yosys to convert VHDL to Verilog
  - Test the VHDL implementation with Chisel
  - Same tester as the one for the Chisel test
- Show it

Conclusion

- We aim for an open-source digital design and verification framework
- Start is the Chisel HW construction language
- First steps explored with Scala, Verilator, and Yosys
- On-going project on open-source verification
- See: https://github.com/chisel-uvm
- Joining the effort is very welcome