OpenPhySyn: An Open-Source Physical Synthesis Optimization Toolkit

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***Abstract*—Physical synthesis is a crucial phase in modern EDA design due to the challenges in achieving timing closure. Many approaches have been presented to solve different design problems and violations, such as buffer-insertion, gate-sizing, pin-swapping, gate-cloning, and logic transformations; each approach has different overhead costs in terms of area, power, and run-time. This paper describes OpenPhySyn, a new open-source EDA kit that implements and enhances different physical and logical design algorithms to resolve design violations and perform timing closure. The tool integrates seamlessly with standard EDA flows and tackles different types of violations with minimal human interference and reduced area overhead. Testing OpenPhySyn against different benchmarks with different characteristics from 46 violations up to 1200 violations showed that the tool solved most of the presented violations with only a 4% average increase in the design area.**

***Index Terms*—physical synthesis, optimization, buffering, resizing**

I. Introduction

Solving electrical and timing violations is a challenging problem in modern digital design. The problem complexity increases significantly with the shrinkage of technology nodes and the increase of interconnect delay [1] [2] [3]. Common approaches for solving design violations include buffer insertion, gate-sizing, and pin-swapping. Additionally, resolving the design violations entitles a significant increase in the design area and power due to the added or upsized cells.

Several approaches have been well-studied to find optimal solutions, such as the classical van Ginneken dynamic buffering approach [4] that uses a dynamic programming approach to find the optimal buffer tree for a given pin. Karandikar *et al.* explains a gate-resizing approach to solve different types of electric violations [5]. Additionally, other techniques have been added to optimize the performance of the classical algorithms, such as the approach by Shi *et al.* that decreases the run-time of the van Ginneken buffering significantly [6].

OpenPhySyn [7] is an open-source toolkit that performs various physical and logic synthesis optimizations to solve design violations while minimizing the area overhead as a secondary objective. OpenPhySyn provides an implementation for many of the standard optimization algorithms in addition to novel enhancements for the implemented techniques.

OpenPhySyn utilizes modern open-source packages such as OpenSTA [8] for incremental timing analysis and OpenDB [9] for managing the loaded design. The tool also reads and writes using standard LEF/DEF format, facilitating the integration with different EDA flows.

Moreover, OpenPhySyn is based on a flexible infrastructure that facilitates the implementation and integration of any optimization algorithm through a dynamic modular architecture while providing a comprehensive utility library to speed up the development process and direct the developer's effort to the core logic of the optimization.

In this work, we present the following contributions:

- We present OpenPhySyn, a new open-source physical synthesis optimization framework with the implementation of many classical optimization algorithms and interfaces to integrate with EDA flows.
- We present an overview of the tool's main optimization commands, the tool exports various optimization commands that solve design violations with different techniques.
- We show an outline for the implemented approaches; the tool utilizes different approaches to tackle design violations with minimal area overhead.
- We evaluate our tool against different EDA benchmarks and show the optimization results while comparing against the existing OpenROAD flow [10].

The rest of this paper is organized as follows. Section II presents the tool flow, Section III shows the experimental evaluation, and we conclude in Section IV.

II. OpenPhySyn Overview

A. OpenPhySyn Architecture

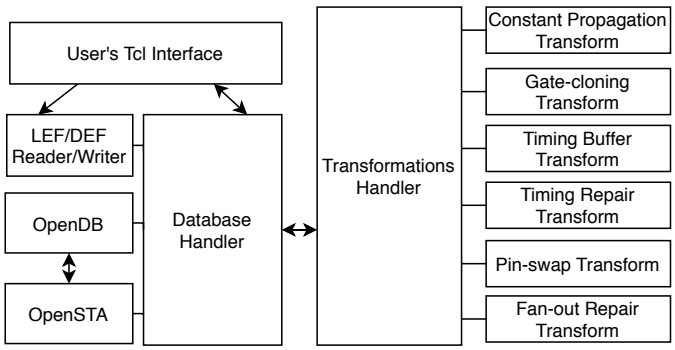

Fig. 1: Overview of OpenPhySyn Architecture

As shown in Fig 1, OpenPhySyn utilizes a modular architecture to facilitate extensibility and development. Conforming to the EDA tools standards, the tool provides a scriptable **Tcl interface** to process the design and perform various optimizations; the tool packages a broad set of optimization commands, with global optimization commands and more granular optimization commands for experienced users. The **LEF/DEF readers and writers** provide the user with an interface to read and write design files; the interface uses OpenDB's Si2 LEF/DEF parsers internally to process the design into the database. The **Transforms Handler** provides a modular interface for any optimization implemented in the tool. The handler has a dynamic interface to allow loading any optimization implementation in compile-time or run-time. OpenPhySyn uses its internal Transforms Handler to implement an essential set of optimization algorithms; the optimizations can be easily chained and evaluated. The **Database Handler** is the primary layer in OpenPhySyn's architecture. Firstly, it provides a generic interface to edit the design structure with access to different components. Secondly, it provides an interface to query the incremental timers or analyze various design violations giving the user the flexibility to interchange the design database or the incremental timer with any other third-party tools with minimal changes to the optimization algorithms. Thirdly, it provides a broad set of utilities and helpers to facilitate the development of any new algorithm. Finally, it encompasses a Boolean logic simulator that can extract and analyze any standard cell's logic functionality and perform Boolean simulations used in logic optimization. Fig. 2 summarizes the different modules provided by the database handler to provide the mentioned functionality:

- **Design Utilities & Helper Algorithms:** provides a broad set of algorithms and utilities to interface with the loaded design and implementation for common useful algorithms. The provided built-in optimizations are based on the given utilities, demonstrating the reuse of the shared infrastructure between different transforms
- **Steiner Tree Heuristics:** provides methods to construct and use Steiner trees using the estimation heuristics from the FLUTE package [11]. The constructs provide different computation methods for the Steiner trees, such as the total wire length estimation and total capacitance/resistance for the given wire trees.
- **Constraints & Violation Checkers:** provides a set of different flexible functionalities that can detect and highlight different types of violations in the design. The checkers are used by the built-in optimizations to extract the targeted violations to fix while supporting variable constraints provided by the user.
- **Boolean Simulator:** provides a Boolean evaluator that uses the Boolean functions defined in the liberty file to simulate the design's logic functionality. The simulator can analyze the different functionality of each cell, extract the liberty cells for a given cell type (buffers, inverters, AND gates..etc.), or simulate any given input values to the cells.
- **Timer (OpenSTA) and Parasitcis Engines Interfaces:** provides a timer and parasitics interface to interface with any provided time or parasitics extractor. The interface provides an interface to perform any timing-based computations through OpenSTA internally, or query the parasitic information for different design components.
- **Legalizer Interface:** provides an interface to integrate a placer to run incremental legalization throughout the optimizations. While OpenPhySyn is not shipped with a built-in legalizer, the optimization commands support the legalization interface allowing the user to easily plugin their placer to do incremental legalization throughout the optimization phases.
- **Database (OpenDB) Interface:** provides an interface to the database infrastructure to load and manipulate the different design data structures. The interfaces provide access to different design blocks implemented by OpenDB without the need for internal knowledge of the database's complexities.

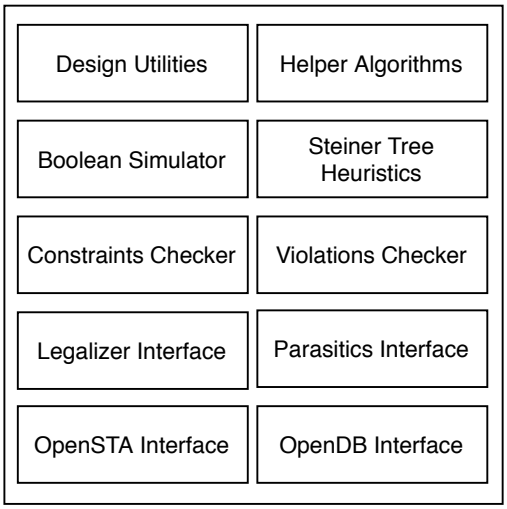

Fig. 2: OpenPhySyn Database Handler modules

B. OpenPhySyn Optimization Transforms

OpenPhySyn aims at tackling design violations with minimal area overhead. Hence, the tool includes a standard set of optimizations that addresses different types of violations while minimizing the added area as a secondary objective. The algorithms use several design optimization techniques such as buffer-insertion, gate-sizing, commutative pin-swapping, gate-cloning, and logic-transformation. The tool exports commands for the following optimizations and utilities included in by default in the tools' source code:

- **Buffer library selection**: the approach automatically selects a set of a representative buffer from the library with a given size using the buffer clustering technique by Alpert *et al.* [12]. The algorithm relies on clustering the buffers based on their intrinsic characteristics, resulting in a representative set of buffers to solve the optimization

problems more time-efficiently. The selected buffers are used by further buffering algorithms or exported to be utilized by other optimization flows.

- **Timing-driven buffering**: the optimization performs fast buffer cell insertion [6] across the design to improve timing and solve violations.
- **Logic transformation**: the optimization performs logic transformation to replace different blocks from the designs with other logically-equivalent components to solve violations in a more area-efficient manner. Fig. 3 shows an example of the logic transformations performed to optimize the design while using the logic function to reduce the area overhead.

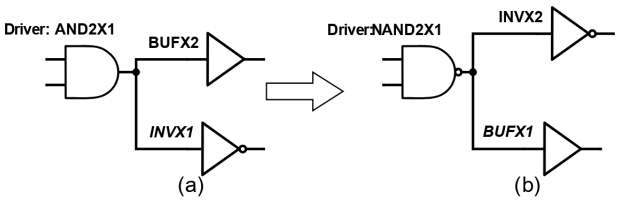

Fig. 3: Example of optimization of the block (a) through logic transformations to block (b) while keeping the logic functionality intact.

- **Fan-out repair**: the optimization performs a fast pass to break down large fan-out trees through buffer tree insertion to distribute the fan-out solve maximum fan-out violation.
- **Commutative pin swapping**: the optimization utilizes the Boolean simulator provided in the database handler to extract logically-commutative pins across the critical design paths followed by applying pin-swapping to enhance the path delays without affecting the logic functionality of the circuit.
- **Constant propagation**: the optimization performs DFS-based constant propagation across the design to eliminate redundant logic and save area. The optimization can be run after the logical synthesis, especially in hierarchical designs, to reduce the cell area by eliminating unnecessary cells.
- **Gate cloning**: the optimization performs load-driven gate-cloning to reduce the load for cells driving high capacitance [3] [13].
- **Comprehensive timing repair**: the comprehensive optimization utilizes the previously described approaches: buffer selection, buffer insertion, gate-sizing, pin-swapping, gate-cloning, and logic transformation through a composition strategy to solve electrical and timing violations efficiently. The optimization selects one or more techniques to solve each violation based on the state of the design. The exported command provides different control flags to customize the optimization's behavior as needed, such as controlling the pessimism level for optimization, specifying the minimum accepted gain, enabling or disabling different techniques, and run-time versus quality trade-off. Additionally, the optimization supports using a detailed placer interface to perform incremental legalization during the optimization if the user links any third-party placer.

C. Optimization Modes and Violation Types

OpenPhySyn optimizations tackle different types of violations, including electrical violation (caused by capacitance and transition limits), hold and setup violations (caused by path delays), and fan-out violations (caused by high fan-out pins). To accommodate for parasitics and estimation error, OpenPhySyn optimizations support pessimistic, ideal, and optimistic modes. This allows the optimization to meet tighter constraints, increasing the design tolerance for violations introduced in further flow stages. Additionally, the tool accommodates for more user-defined constraints such as the maximum-utilization or custom dont-use cells.

D. OpenPhySyn Flow Integration

OpenPhySyn is designed and structured to integrate seamlessly with other EDA flow tools, avoiding the reliance on any custom file format or uncommon structures. As mentioned earlier, the tool provides flexible layers to interface with an incremental timer or structural design database. Additionally, the tool provides an interface to integrate placement tools to enable incremental legalization, which is supported with different modes by the provided optimization. Moreover, the tool supports different modes for wire parasitics estimation: providing average custom wire parasitics, automatic extraction for average wire parasitics from the LEF file, or interfacing with any external parasitics engine. By default, the wire length is estimated using Steiner trees [14] from FLUTE package [11] and used throughout different optimizations.

III. Evaluation

A. Setup

For the experimental evaluation, we selected six designs from different fields with different sizes and characteristics. We ran our tests using the Nanagate 45nm technoloy [15]. We used Yosys [16] and ABC [17] for the logic synthesis, followed by OpenROAD [10] for floorplanning and placement. The parasitics were estimated from the third metal layer in the LEF file. We passed the placed designs to OpenPhySyn to perform the various optimizations to solve timing and electrical violations followed by a final legalization and evaluation phase while comparing our results against OpenROAD's optimization flow using the same setup conditions. The following Table I gives the initial state of the chosen benchmarks after placement listing their respective number of cells, area in micrometers, clock period in nanoseconds, the total number of transition violations, total number of capacitance violations, worst negative slack in nanoseconds, and total negative slack in nanoseconds.

Design	# Cells	AREA	CLK	TRNS	CAP	WNS	TNS
gcd	386	438	2	0	20	0.0	0.0
d_node	11482	21671	7	11	46	0.0	0.0
aes	16331	19056	5	49	213	0.0	0.0
ibex	25337	42510	10	64	177	0.0	0.0
jpeg	79608	102683	4	288	1059	0.0	0.0
swerv	94089	149101	10	383	1203	-273.26	-2514391.5
AVG	**37872.17**	**55909.83**	**6.33**	**132.50**	**449.67**	**-45.54**	**-419065.25**

TABLE I: Initial state of the chosen benchmarks after placement

B. Results

The given Table II shows the benchmark names, the percentage increase in the design area, the number of transition violations, the number of capacitance violations, worst negative slack in nanoseconds, and total negative slack in nanoseconds when optimized by OpenROAD's flow compared against OpenPhySyn's optimization's flow.

As shown from Table II, OpenPhySyn gives superior results where it solves most of the presented violations with an average 4% area overhead compared to OpenROAD's flow that adds an average 19% area overhead while failing to solve many of the presented violations.

IV. Conclusion and Future Direction

We presented OpenPhySyn, a novel open-source physical synthesis optimization kit that tackles modern EDA timing closure challenges. The tool utilizes a modular architecture and provides an infrastructure to facilitate the development of physical optimizations. OpenPhySyn is designed to work seamlessly within a full EDA flow by using standard input and output formats for the processed design. Moreover, OpenPhySyn packages and enhances many of the standard EDA optimization algorithms. Additionally, OpenPhySyn performs intelligent compositions for the packaged algorithms to optimize the loaded designs efficiently. We evaluated the optimizations' quality against different benchmarks and compared them against OpenROAD's optimization flow showing superior results in both the area overhead and the number of solved violations. Our future work is to extend OpenPhySyn to design and implement more EDA algorithms to solve more complex violations with better efficiency. We also plan to integrate reinforcement learning models for a more intelligent composition and computation for the different optimization algorithms. Finally, we plan to provide more built-in integrations with other third-party tools like placers and parasitics engines.

V. Acknowledgment

OpenPhySyn is available open-source in the public domain under the BSD-3-Clause License accessible at https://github.com/scale-lab/OpenPhySyn. The tool is tested on Linux and macOS platforms using different commercial libraries, including 65nm and 14nm technology nodes.

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	Original OpenROAD Flow					OpenPhySyn Flow				
Design	**△AREA (%)**	**TRNS**	**CAP**	**WNS**	**TNS**	**△AREA (%)**	**TRNS**	**CAP**	**WNS**	**TNS**
gcd	13.70	0	0	0.0	0.0	9.59	0	0	0.0	0.0
d_node	13.14	1	4	0.0	0.0	2.82	0	0	0.0	0.0
aes	35.60	0	0	0.0	0.0	2.95	0	0	0.0	0.0
ibex	12.34	0	0	0.0	0.0	3.82	0	0	0.0	0.0
jpeg	19.89	0	0	0.0	0.0	0.42	0	0	0.0	0.0
swerv	18.76	2	17	0.0	0.0	4.68	0	1	0.0	0.0
AVG	**18.91**	**0.50**	**3.50**	**0.0**	**0.0**	**4.05**	**0**	**0.17**	**0.0**	**0.0**

TABLE II: Evaluation for different violations and area overhead when using OpenPhySyn compared to OpenROAD's optimization