An Automatic Schematic Generation Tool for SPICE Netlists

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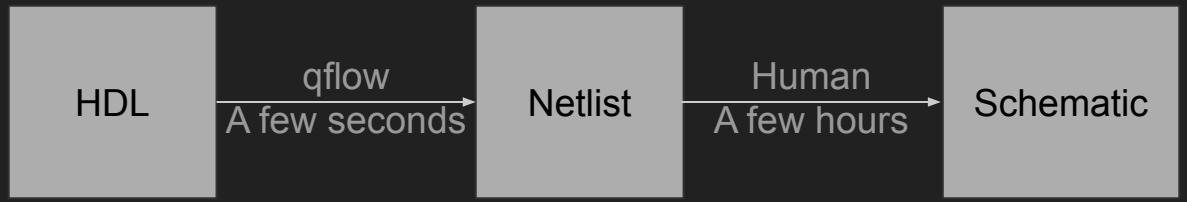
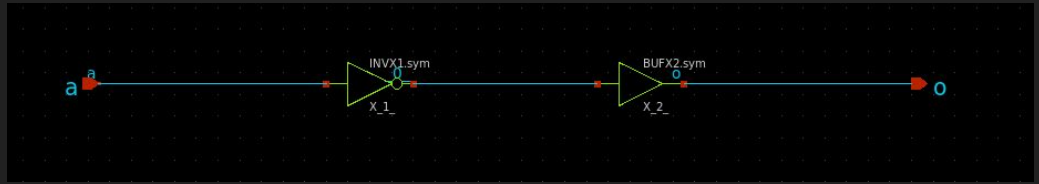
Goals



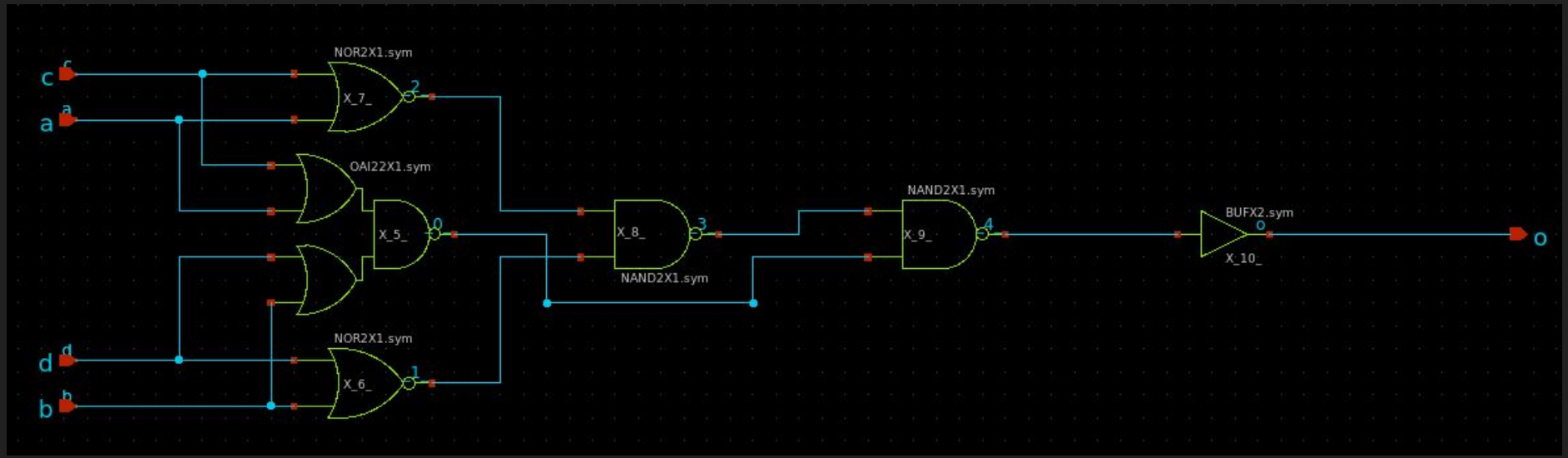
Goals (cont.)

- Be useful for manual repairs to a circuit
- Netlist created by a schematic tool needs to be useful and very similar to the input
- Doesn’t need to be perfect
- Support open source schematic entry tools
  - KiCad EESchema
  - Xschem

Samples

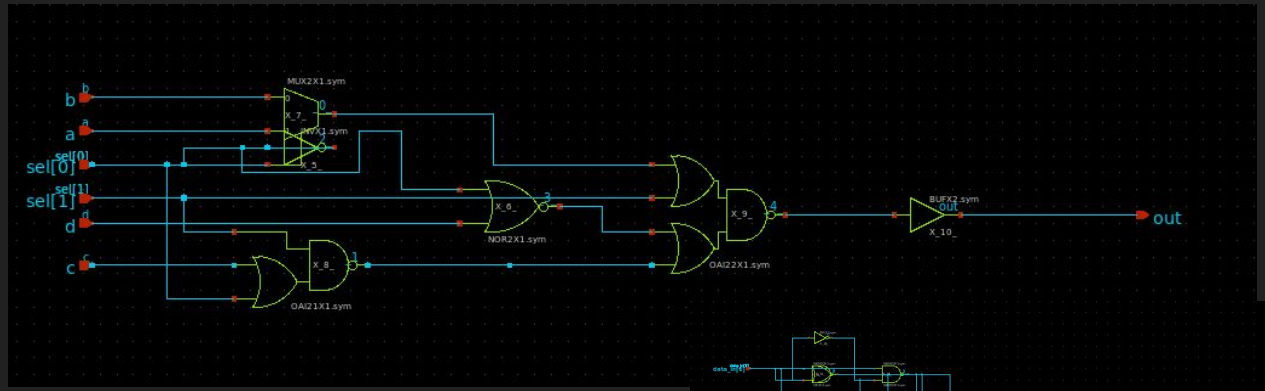


Basic

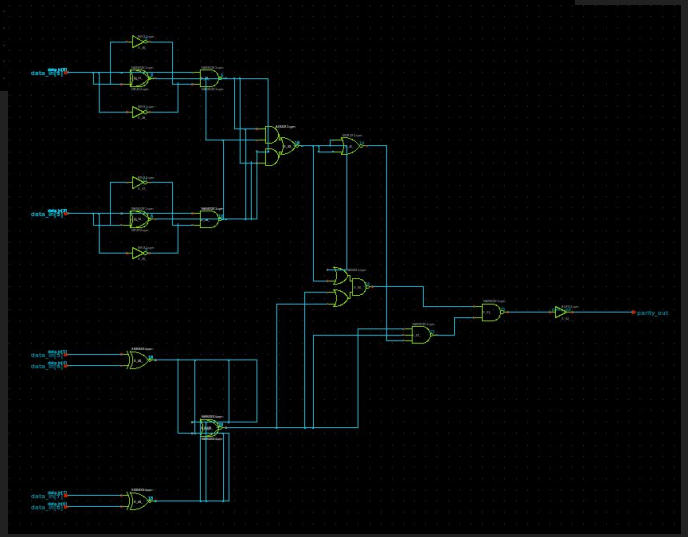


Medium

Samples

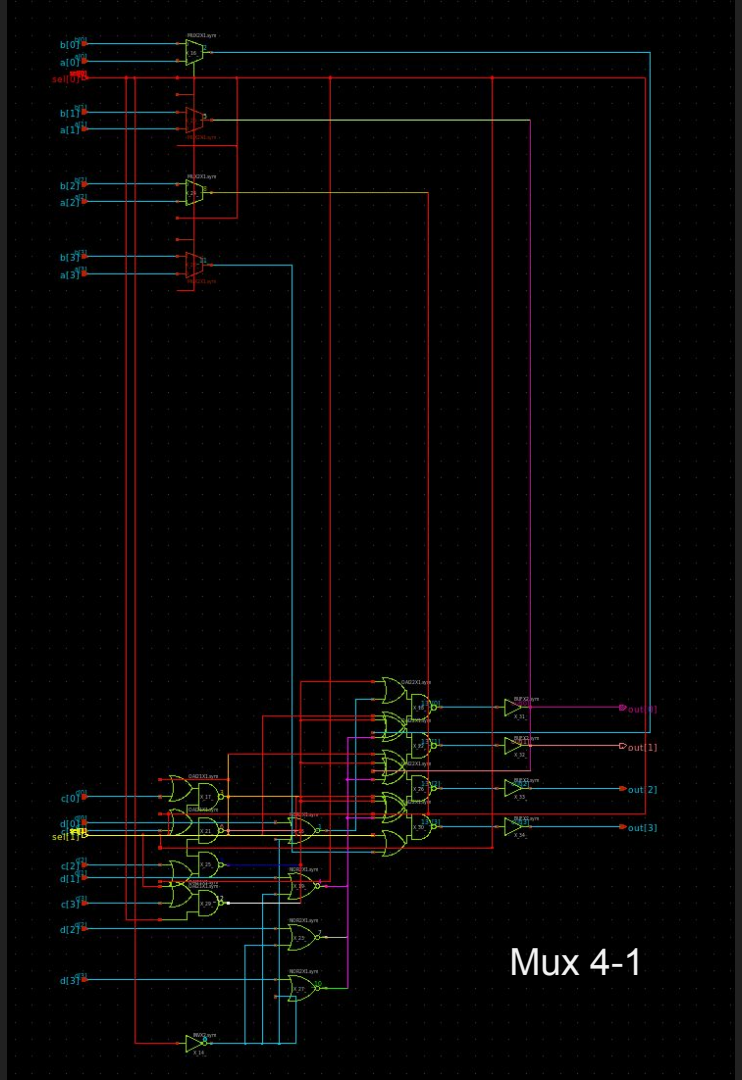


Medium Mux

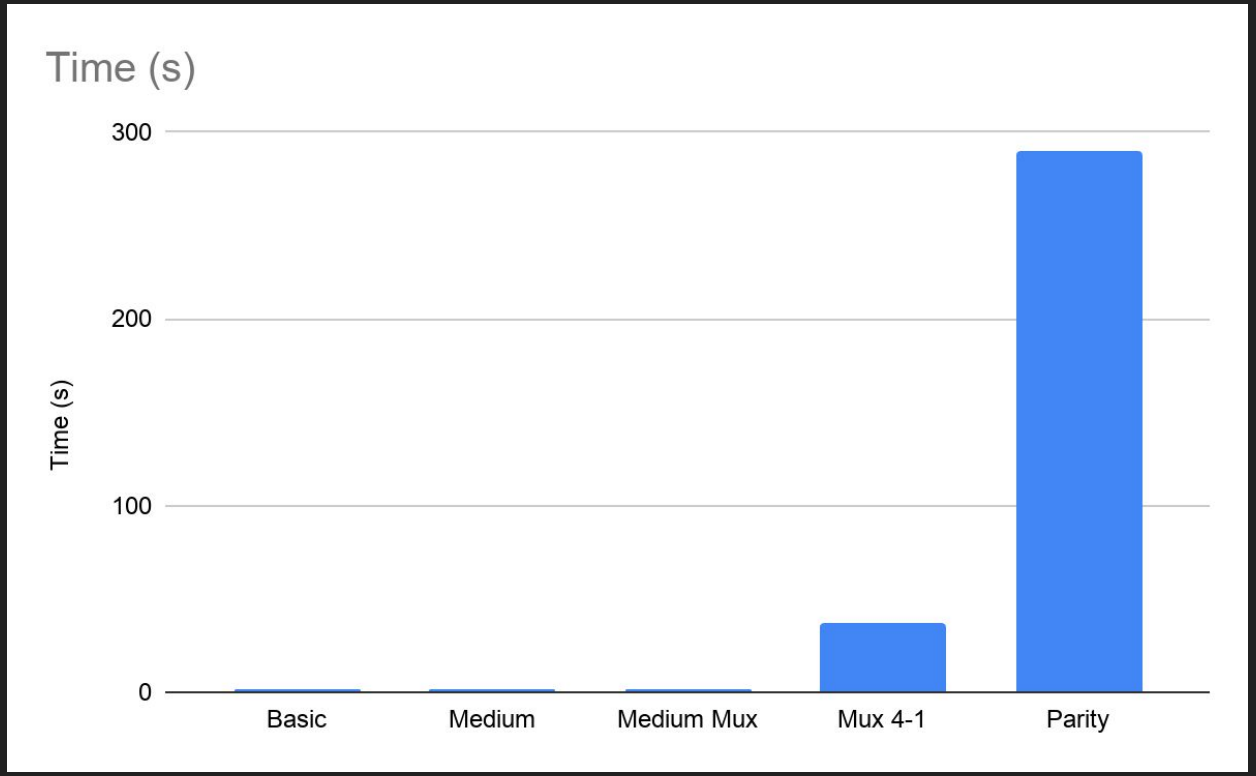


Parity

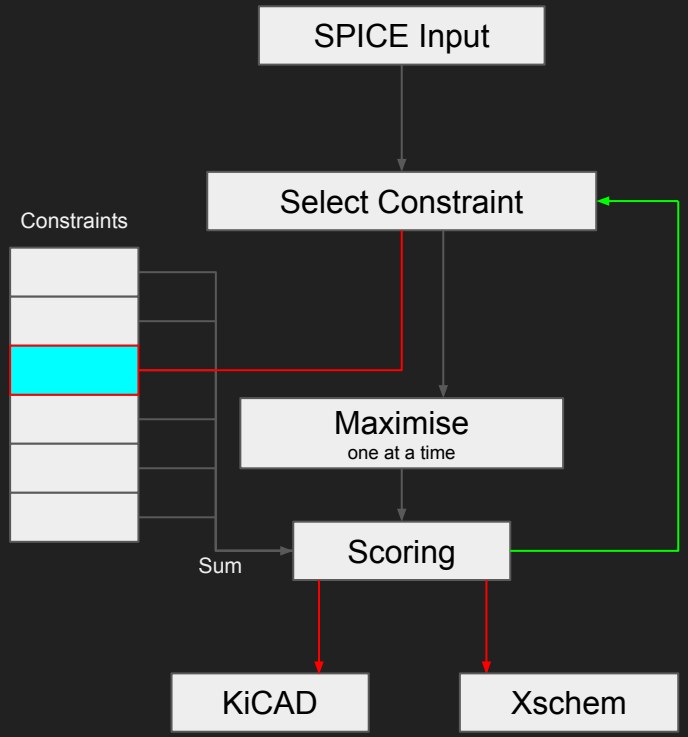
Samples


b[0]
a[0]
sel[0]
b[1]
a[1]
b[2]
a[2]
b[3]
a[3]
c[0]
d[0]
sel[1]
c[2]
d[1]
c[3]
d[2]
d[3]
out[0]
out[1]
out[2]
out[3]
Mux 4-1

Performance



Algorithm


SPICE Input
Select Constraint
Constraints
Maximise
one at a time
Scoring
Sum
KiCAD
Xschem

Other Applications

- Robust Python library
  - Reading netlists and symbol libraries
  - Writing schematics
- Schematic interoperability
  - A tool doesn’t need to write a full schematic to a universal form, could use a netlist with additional metadata

Future Work

- Further optimization
  - Significantly larger schematics take much longer to run
- Potential to improve overarching algorithm
  - Experiment with tree based refinement
- Better & more constraints
- Analog schematics
  - First steps are on GitHub issues

Acknowledgements

- Tim Edwards
- Mr. Lee & Poolesville High School staff

Thanks for watching!

https://github.com/aidangoettsch/asg