OpenLANE: The Open-Source Digital ASIC Implementation Flow

WOSET 2020

efabless.com

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AUC

Outline

- Introduction
- Macro Hardening Flow
  - Issues and Solutions
  - Synthesis/Design Exploration and Benchmarks
- SoC Integration Flow
  - Issues and Solutions
  - striVe2a
- Final Remarks
  - Future Work

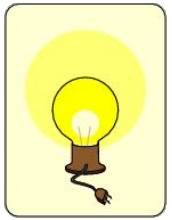
Introduction

Google + skywater TECHNOLOGY

FOSS 130nm Production PDK
github.com/google/skywater-pdk

OpenROAD

theopenroadproject.org



Open Circuit Design

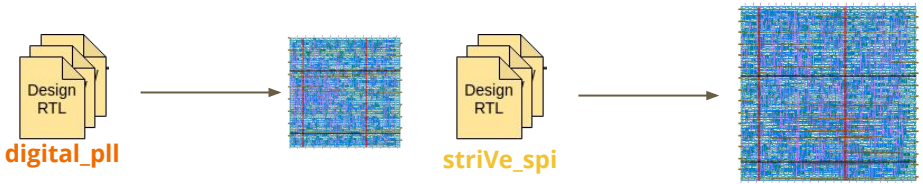
opencircuitdesign.com

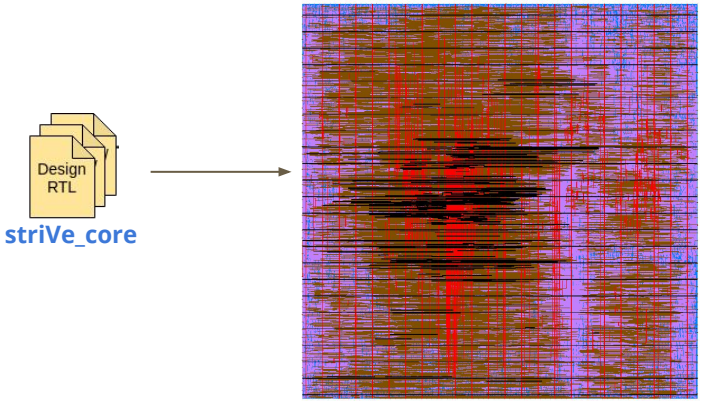
Yosys

github.com/YosysHQ

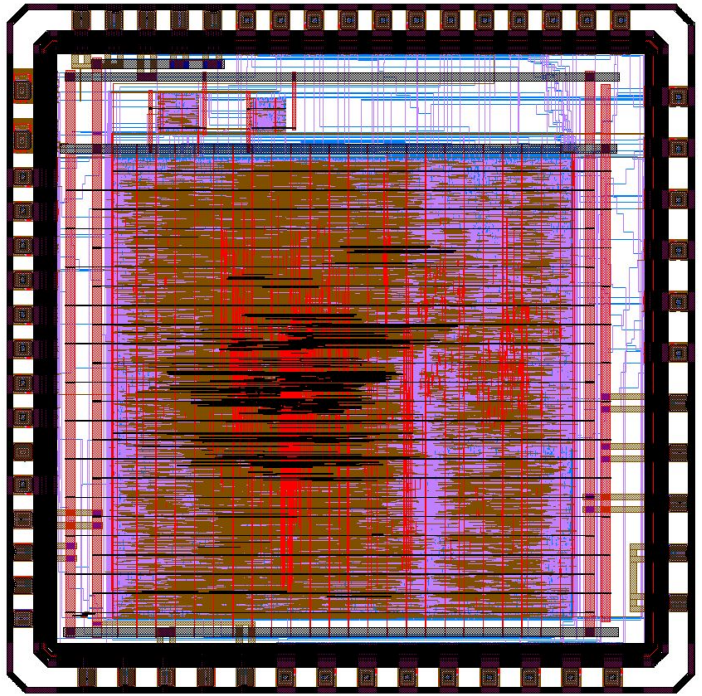
Introduction - Use Cases

1. Macro Hardening

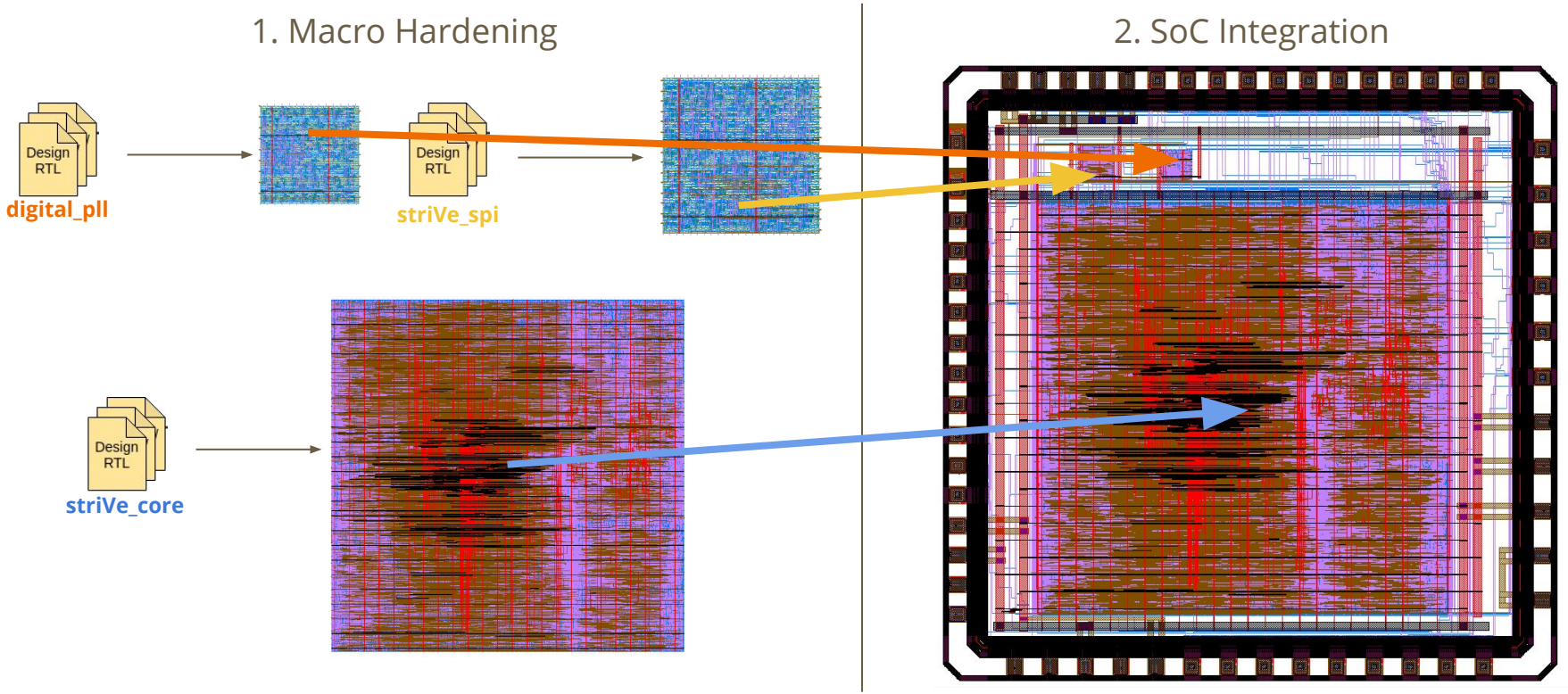




2. SoC Integration

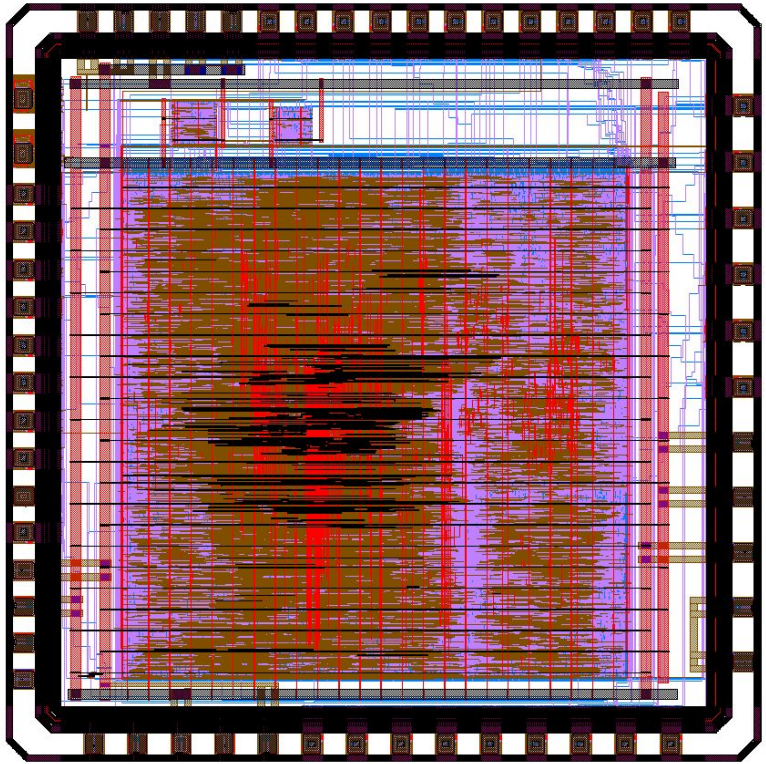


Introduction - Use Cases

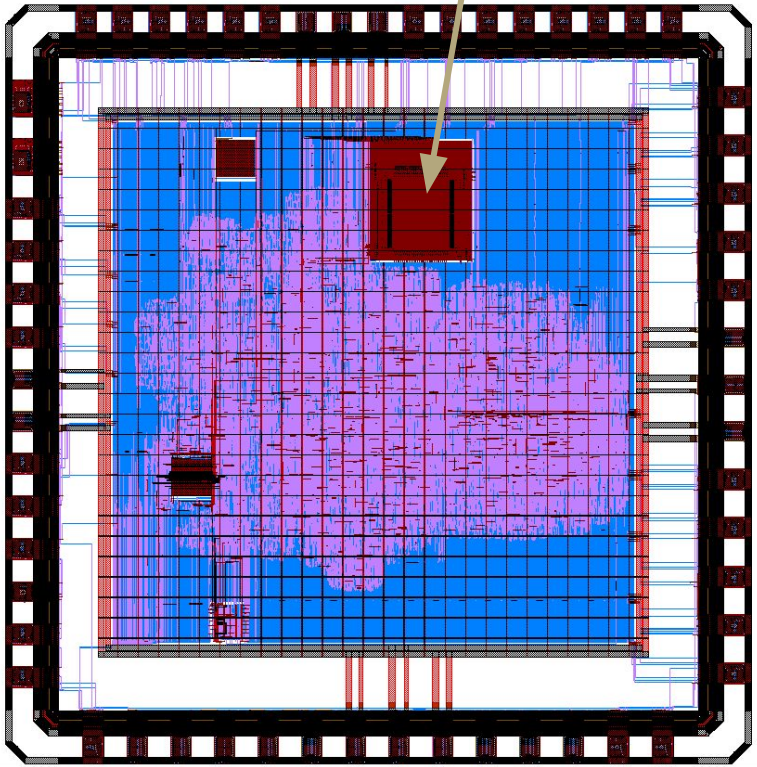


Introduction

striVe

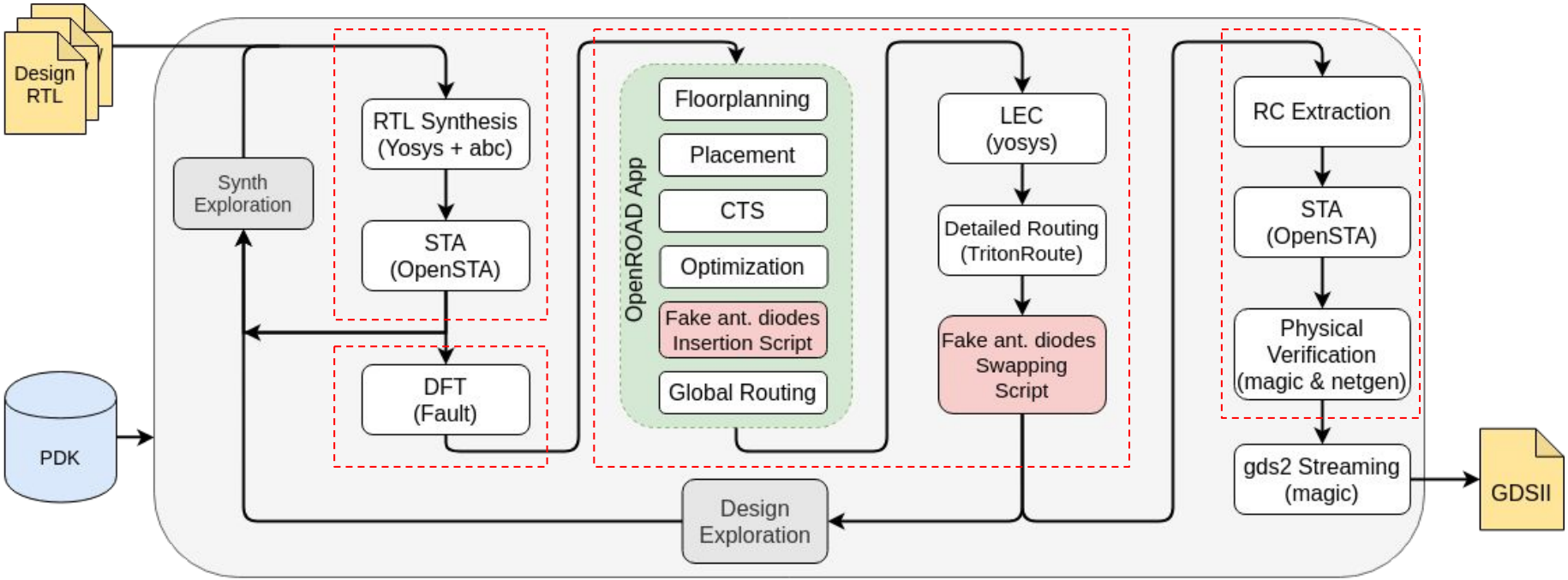


striVe2a *



* SRAM 1KByte Block Compiled by OpenRAM

Macro Hardening



Macro Hardening: Physical Implementation

- Using tools within the OpenROAD Application
- Timing optimizations done using Brown University's OpenPhySyn
- Verification of netlist changes with Logical Equivalence Checks (LEC) using Yosys
- Custom tools:
    - Two additional use cases during I/O pin placement
        - Context-aware I/O placement
        - Specification-based I/O placement
    - Top-level power routing
    - Antenna avoidance methodology

Macro Hardening: Mitigation of Antenna Effects

- Antenna-aware routing
    - Bridging
    - Swapping of routing layers
- Diode insertion

Macro Hardening: Mitigation of Antenna Effects

- ~~Antenna-aware routing~~
  - ~~Bridging~~
  - ~~Swapping of routing layers~~
- Diode insertion

The Antenna Effect - Diode Insertion Strategies

1. Brute Force Solution

Insert diodes on all poly gates (all cell inputs!)

Pros

- Eliminates most antenna violations

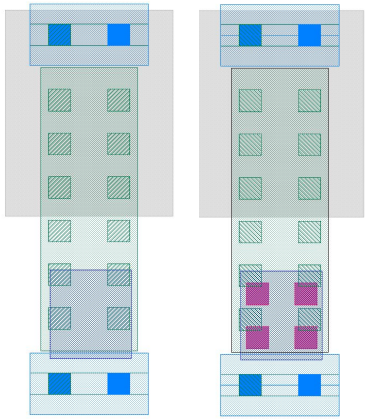
Cons

- Wasted Area - Poses a limit on core utilization
- Power Hungry
- Slower Performance

The Antenna Effect - Diode Insertion Strategies

2. “Fake Diode” Strategy

- Insert fake diodes on all poly gates
- Run an antenna check
- Replace the fake diodes with real diodes as needed



Pros

- Eliminates most antenna violations

Cons

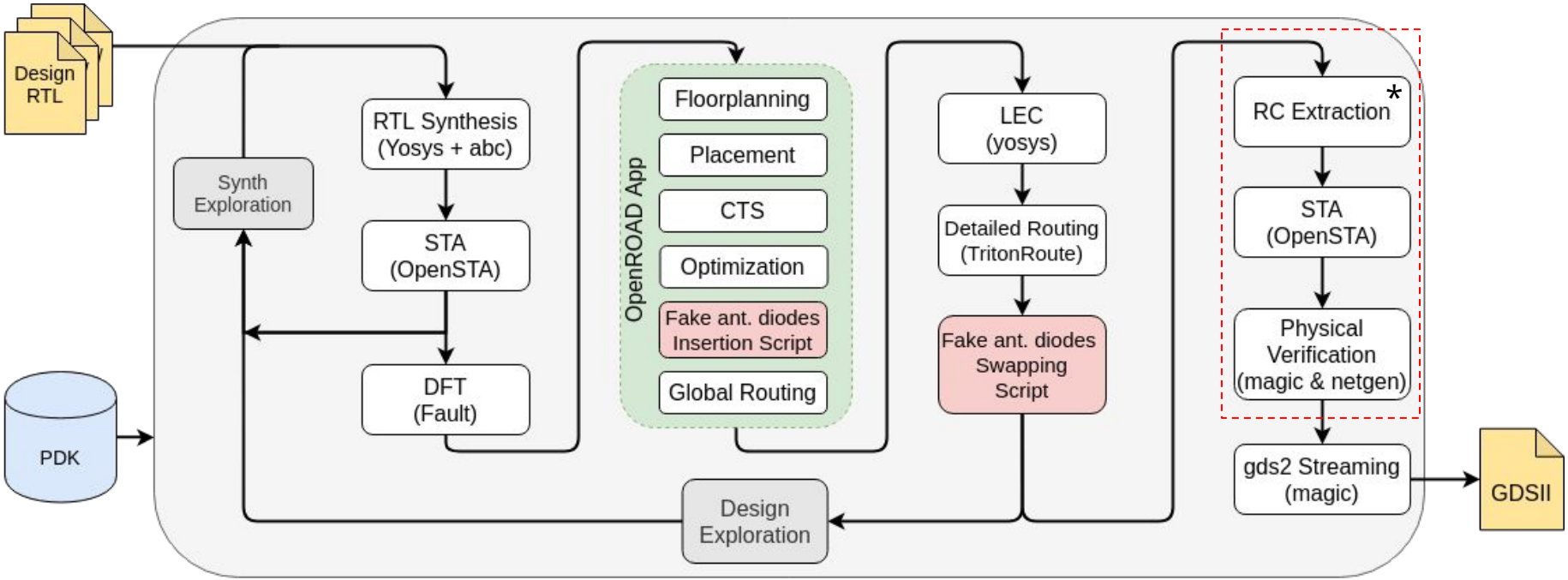
- Wasted Area - Poses a limit on core utilization

The Antenna Effect - Diode Insertion Strategies

3. Antenna-aware Tools

Insert diodes only when needed during global routing (Implemented in FastRoute)

Macro Hardening: Post-routing Evaluations



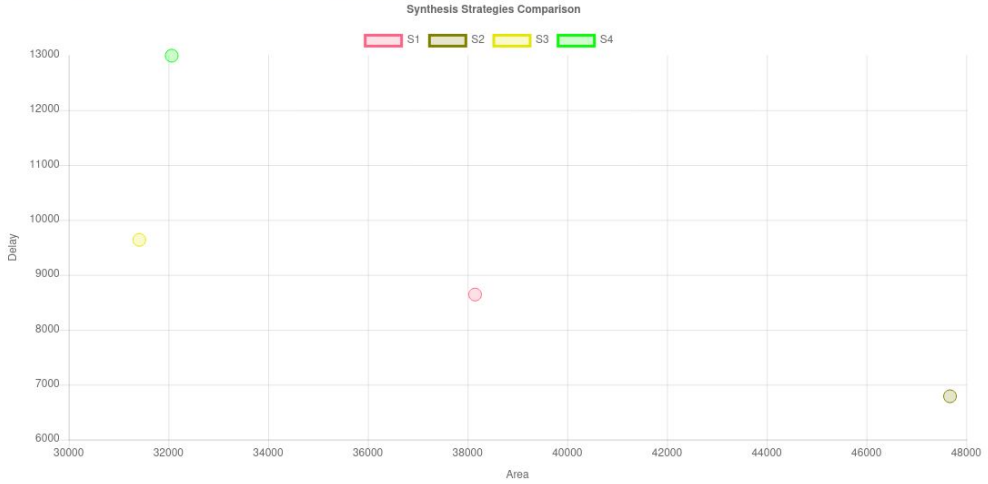
* https://github.com/Cloud-V/SPEF_EXTRACTOR

Synthesis and Design Exploration

- Visual representation of the area-delay relation
- Find the optimal set of values for the configuration parameters

Best Area	Best Gate Count	Best Delay
31415.13	2258	6788.49
-p	-p	-p

Startegy	Gate Count	Area (um^2)	Delay (ps)	Gates Ratio	Area Ratio	Delay Ratio
S1: -p	2583	38150.34	8641.32	1.143	1.214	1.272
S2: -p	3452	47675.73	6788.49	1.528	1.517	1
S3: -p	2685	31415.13	9637.39	1.189	1	1.419
S4: -p	2258	32065.75	12991.97	1	1.02	1.913

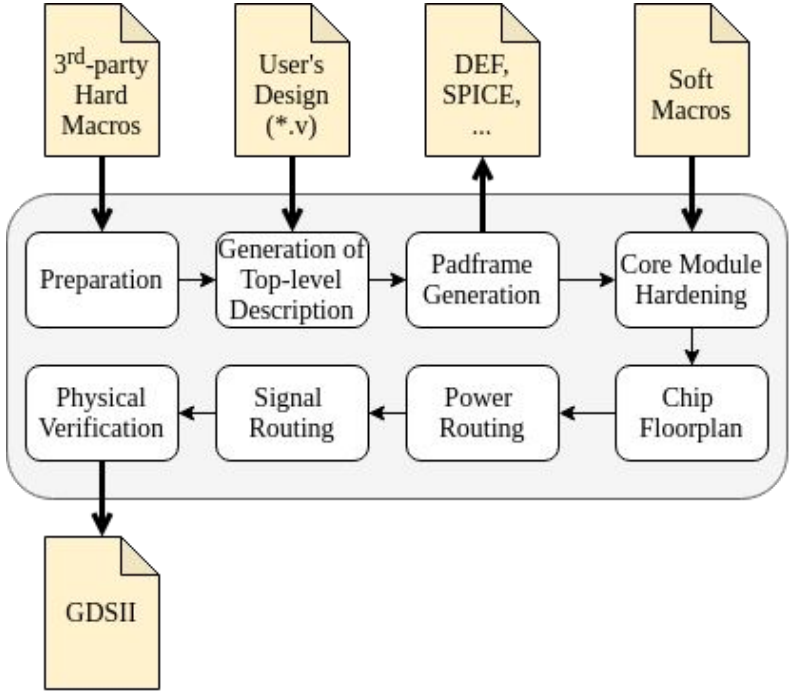


SkyWater Standard Cell Libraries

Standard Cell Library	Usage Notes
High Density (HD)	Stable*, Taped out (striVe, striVe2, openram_tc_1kb)
High Density, Low Leakage (HDLL)	Stable*
High Speed (HS)	Stable*
Low Speed (LS)	Stable*
Medium Speed (MS)	Unstable*
High Voltage (HVL)	Under test
OSU 18T	Under test (striVe3)

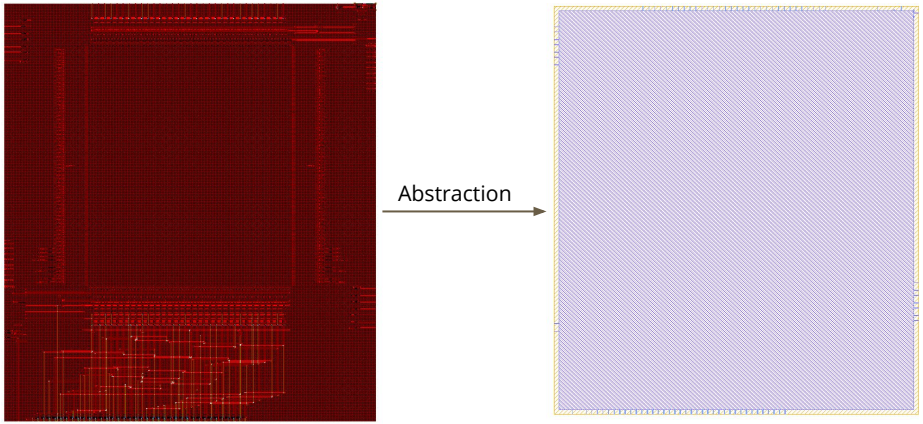
* See benchmarks at https://github.com/efabless/openlane/blob/develop/regression_results/benchmark_results

SoC Integration

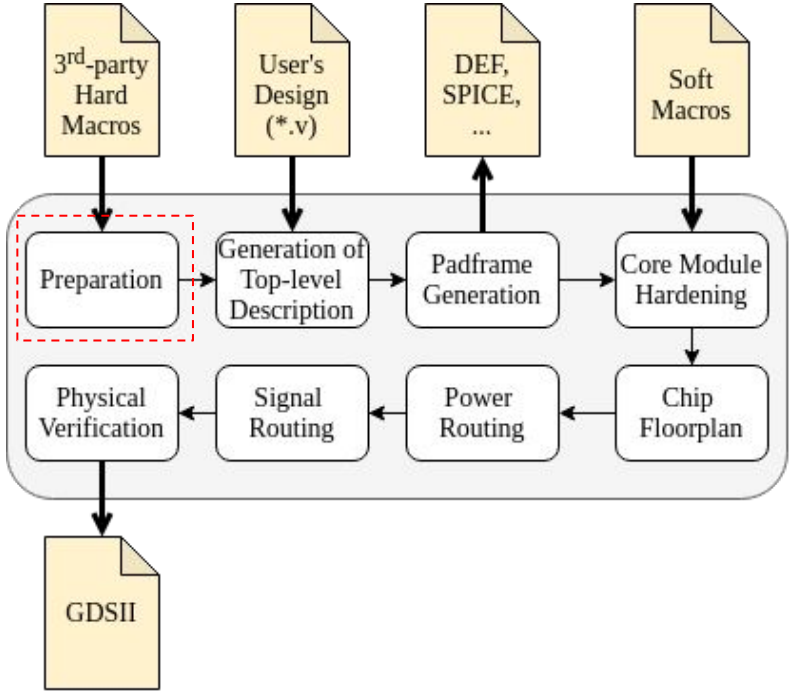


SoC Integration: Preparation

- Utilities to wrap macros to increase their routability (w.r.t available routers)
- Divides and conquers the problems of DRC and LVS

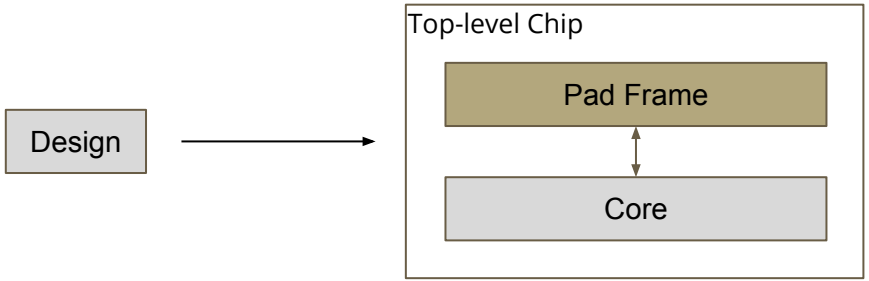


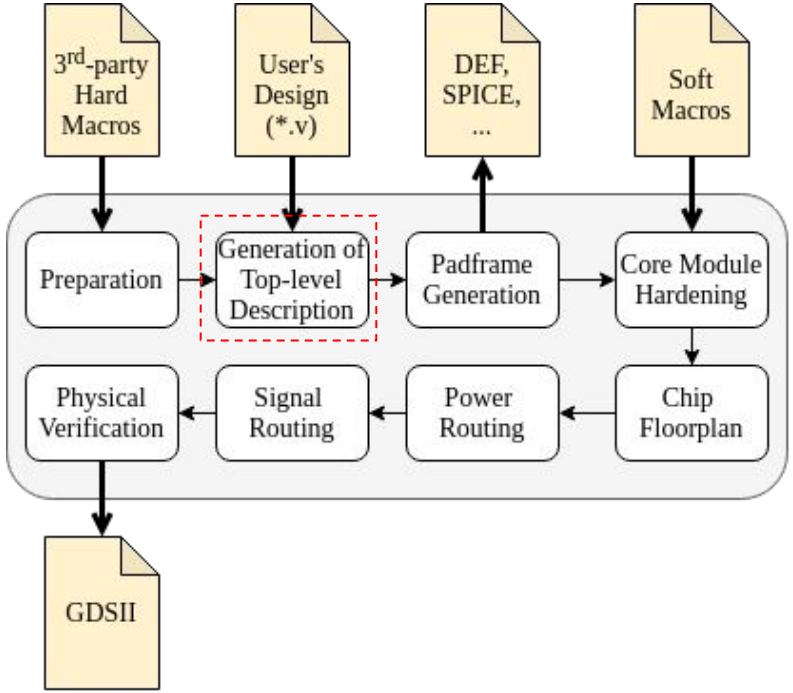
SRAM 1KByte Block Compiled by OpenRAM



SoC Integration: Generation of top-level description

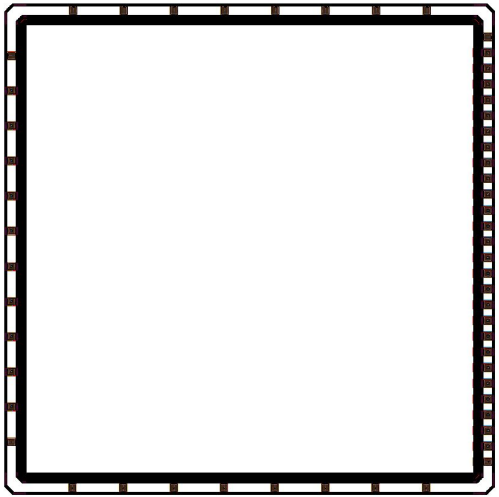
- Optional
- Intended for users unfamiliar with the I/O pads

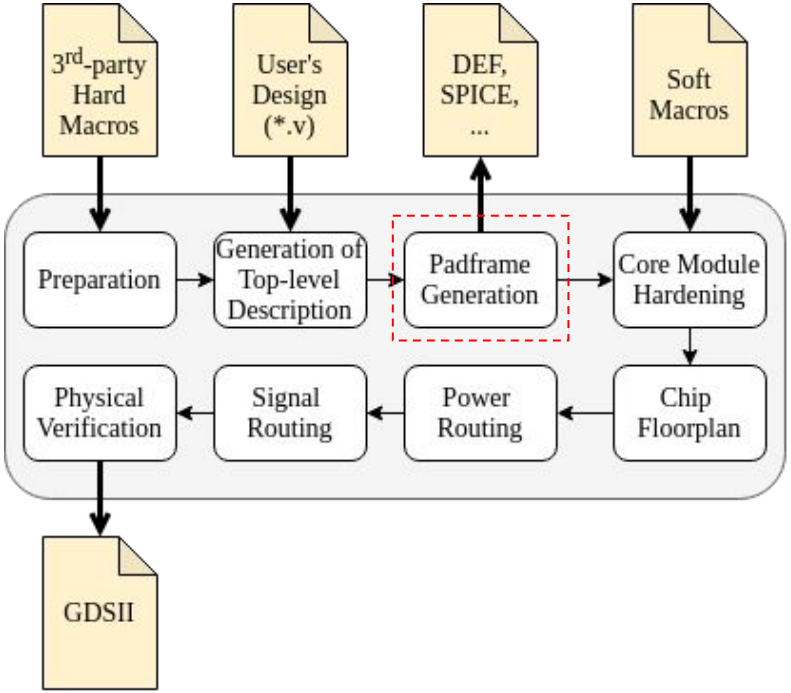




SoC Integration: Pad Frame Generation

- PFG originally by Tim Edwards
- An OpenDB-based version
- Both based on PADRING from YosysHQ



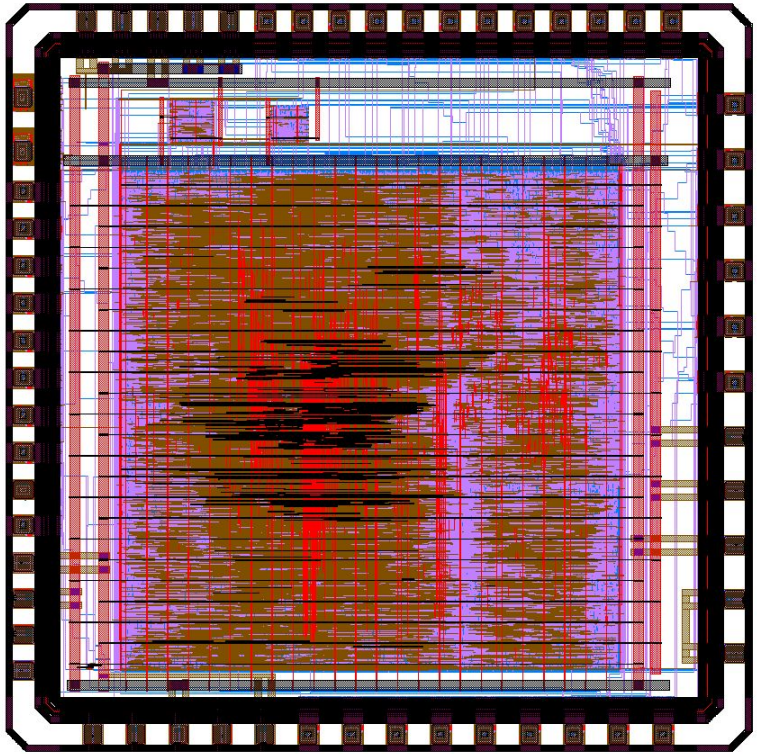


SoC Integration: Learnings from striVe

Issue:

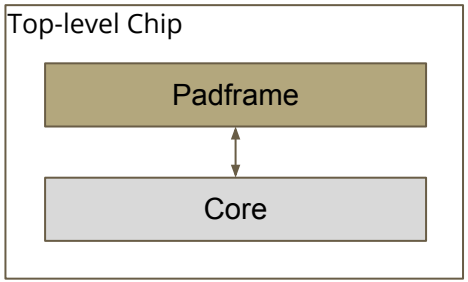
- Macro-to-macro nets causing congestion on the top level
- Sub-optimal I/O pin placement
- Unclean routes → Manual intervention
- Manual power routing

striVe

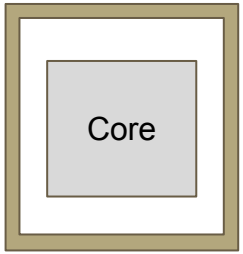


SoC Integration: Recommended Hierarchy

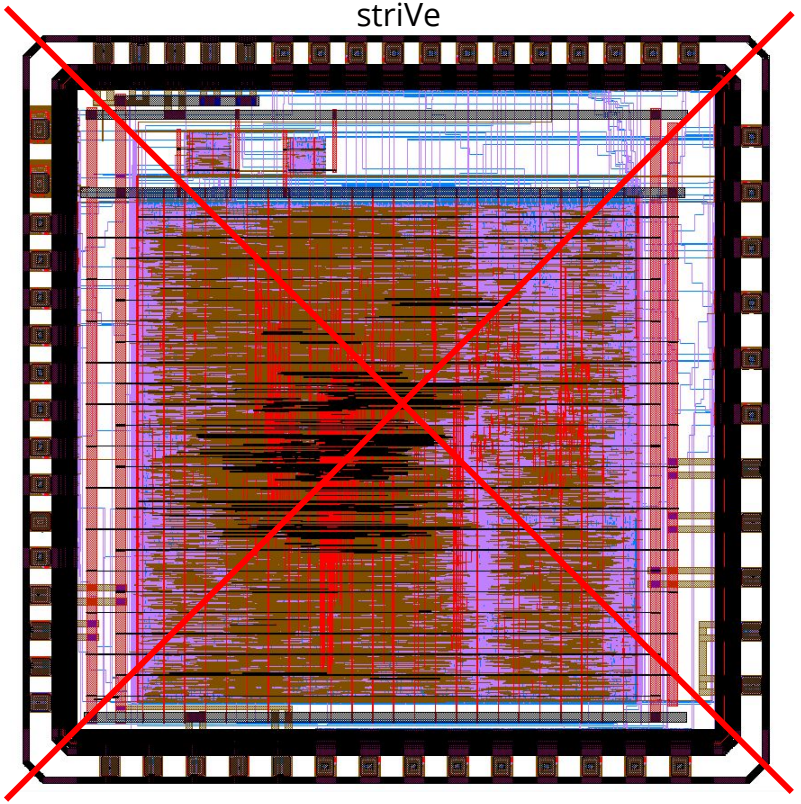
Issue: Macro-to-macro nets causing congestion on the top level



Logical Hierarchy



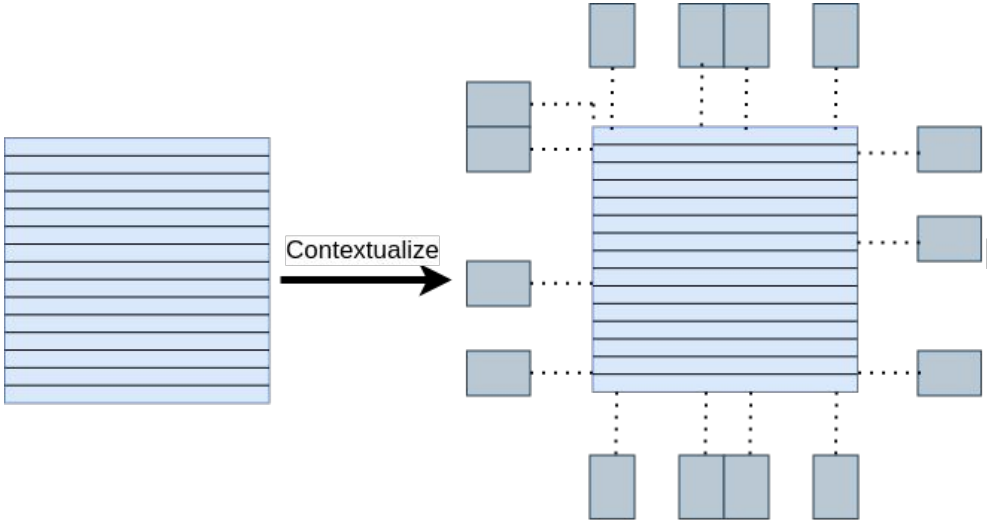
Physical Hierarchy

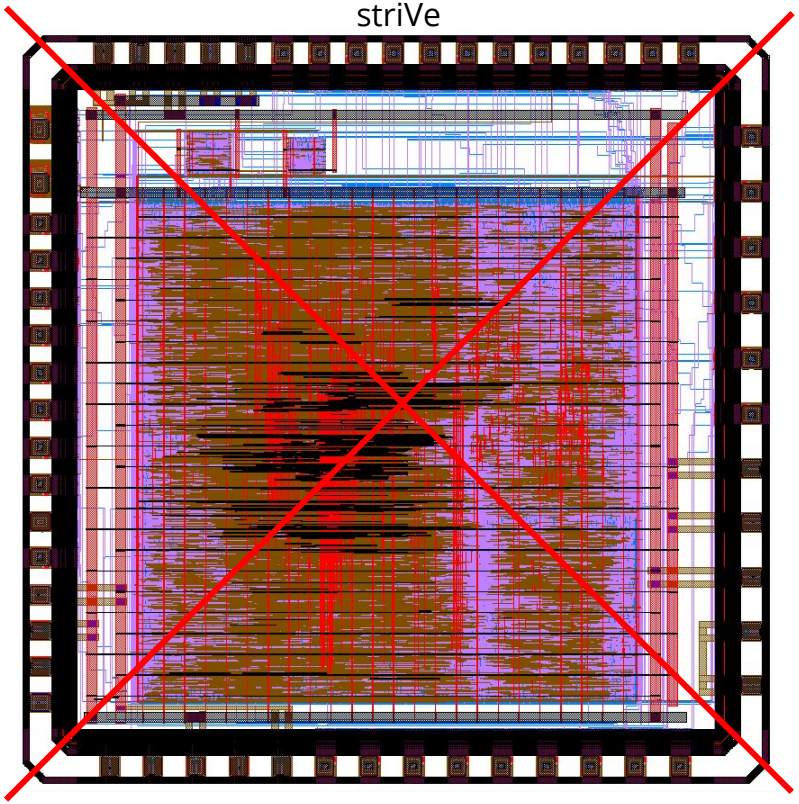


SoC Integration: Context-aware Hardening

Issue: Sub-optimal I/O pin placement

Idea: “Contextualized” Floorplanning

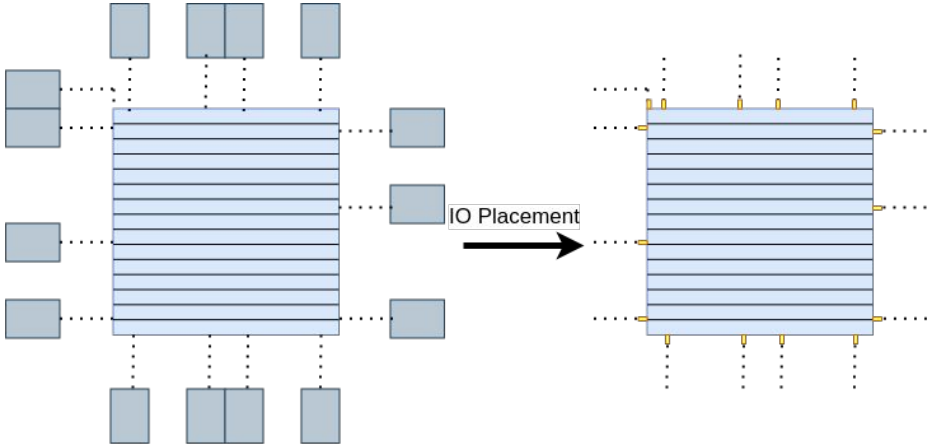


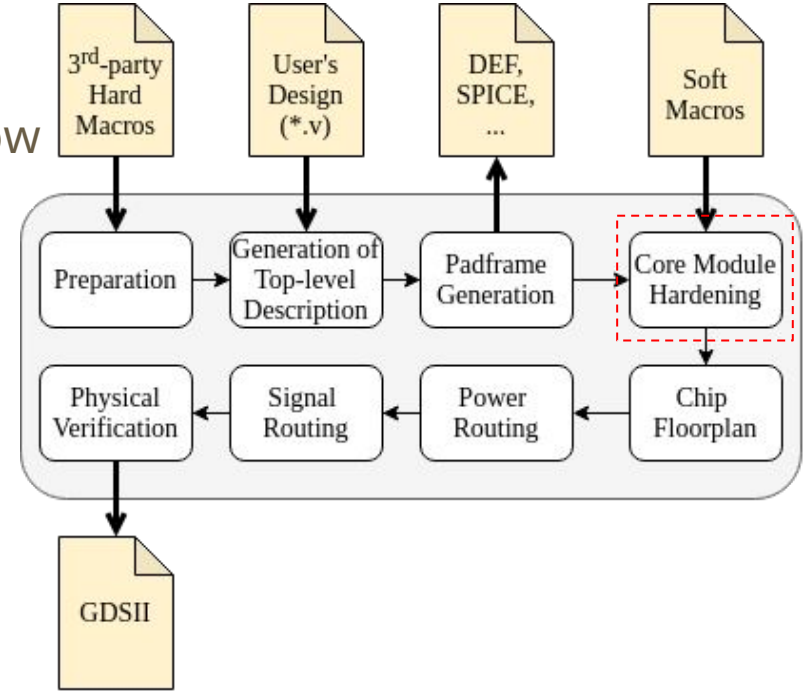


SoC Integration: Context-aware Hardening

Applications:

- Context-aware various steps of the flow
  - E.g., context-aware I/O placement



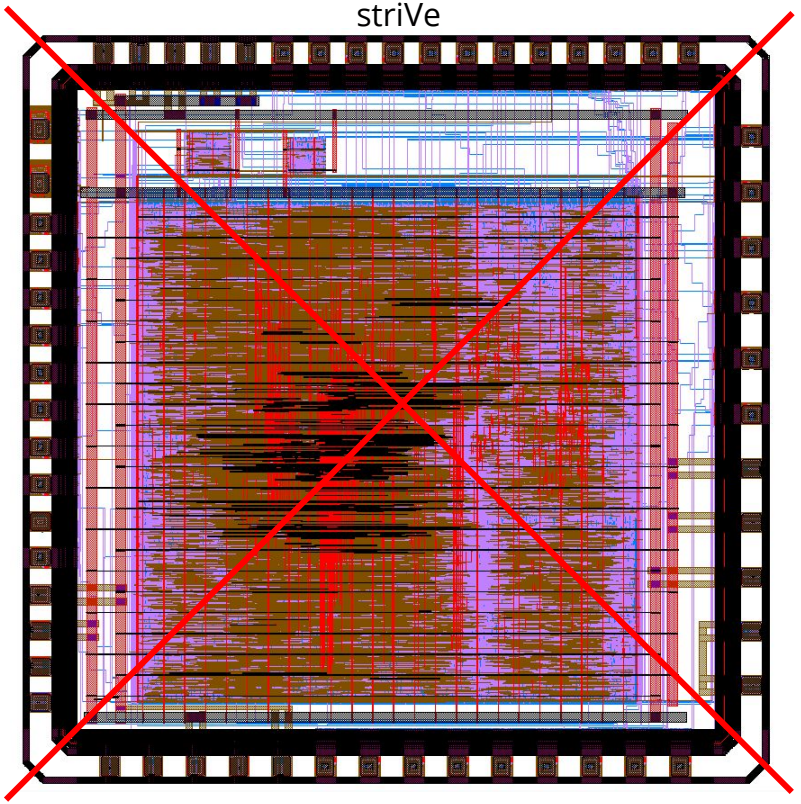


SoC Integration: Power Routing

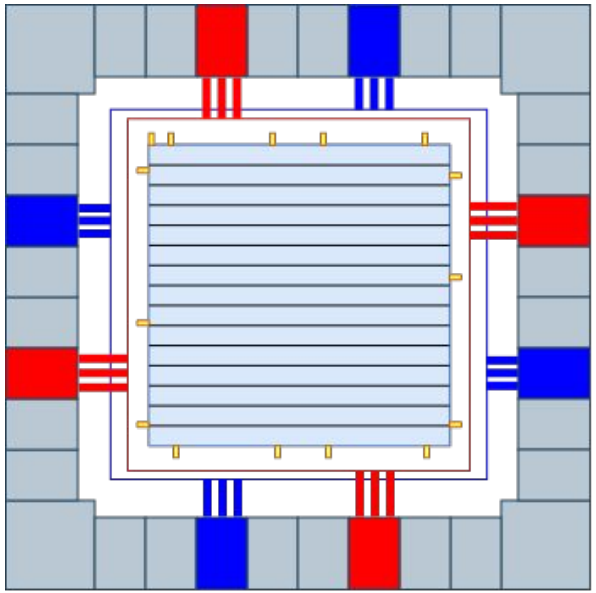
Issue: Manual power routing

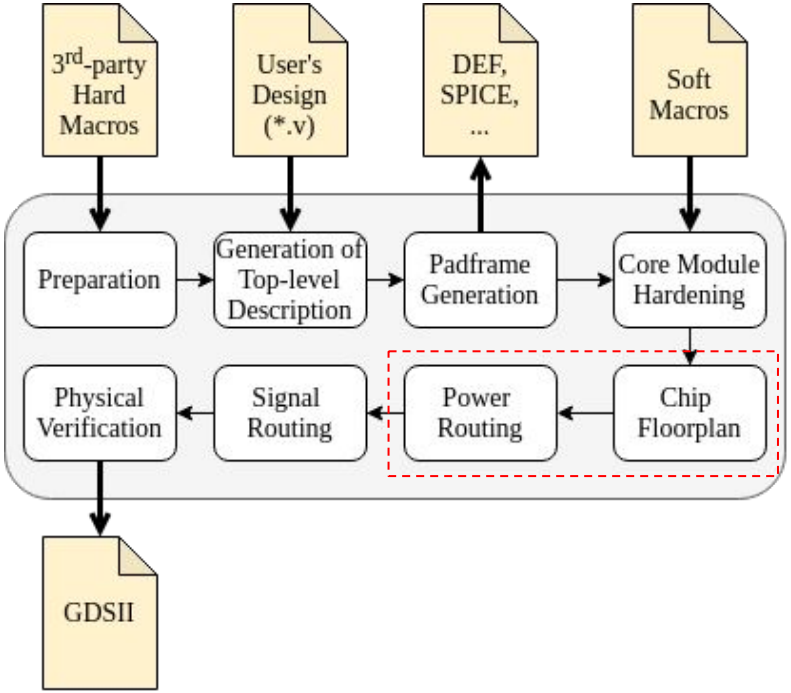
Ideas:

- Recommended hierarchy
- Concentric core rings
- Custom top-level power router
  - Maximize usage of the highest metal layer
  - Maximize the number of vias
  - DRC-correct by construction

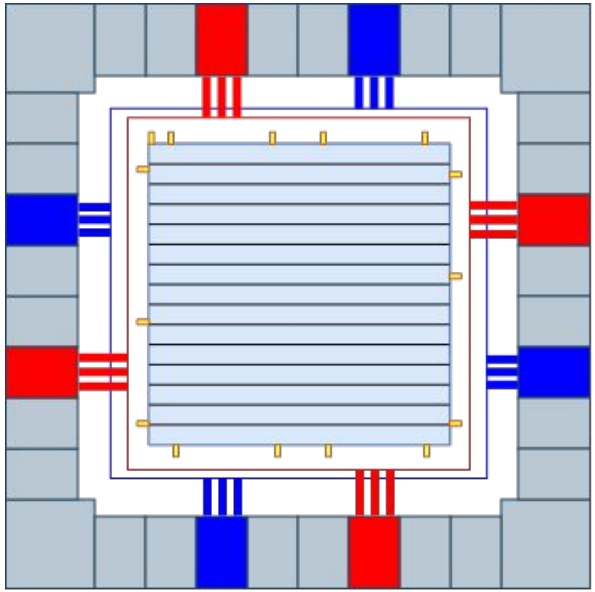


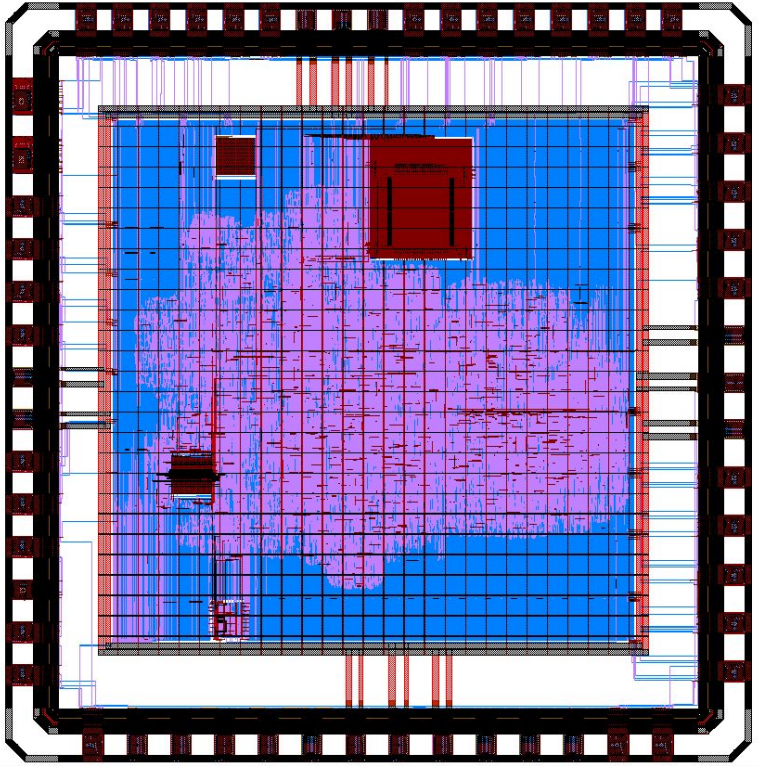
SoC Integration: Power-routed Chip Floorplan





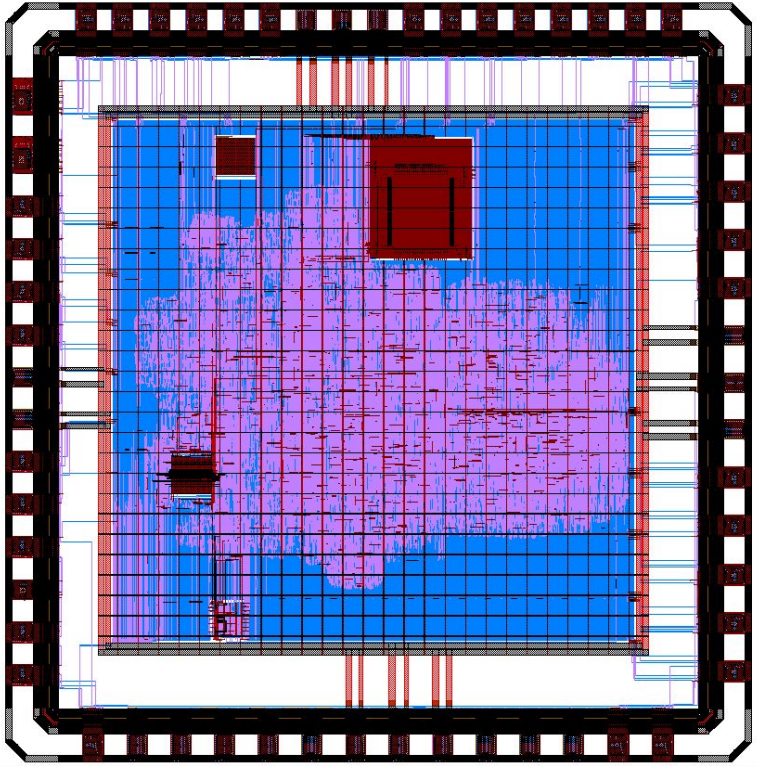
SoC Integration: striVe2a





SoC Integration: striVe2a

- Time to harden everything from scratch and integrate an SoC
    - ~57 mins
- LVS clean
- No real DRC errors seen by open-source tools (e.g., TritonRoute and magic)



Final Remarks

- SoC release is pending the open-source release of the I/O library
- OpenLANE is currently the only open-source flow that can be readily used to almost fully automate chip integration for the open PDK
- Planned to be used for the upcoming public November shuttle

Final Remarks: Future and Current Work

- Work around cons of the recommended hierarchy when it comes to multi-voltage designs
- Adapt some of the SoC features to to work with Caravel
- Target ~0 antenna violations:
  - FastRoute antenna avoidance is not yet perfect

Final Remarks: Acknowledgements

This project would not have been possible without the dedicated work by

Tim Edwards,

Karim Fareed,

Amr Gouhar,

and Mohamed Kassem.

Thanks for listening!