Software Inspired IC Hardware Workflows Using Bazel

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***Abstract*—**

Over the past 20 years a significant amount of development has gone into developer tooling to build software safely, and repeatedly. *Bazel* [1] is an open source build system designed from the ground up to accommodate highly variable language tool chains and massive software builds. This project aims to leverage that very same technology to offer software inspired workflows to build integrated circuits.

In this abstract session, I discuss the open source project `hdl/bazel_rules_hdl` [2] which aims to use *Bazel*, *OpenROAD* [3], *Yosys* [4] and other open source tools to build a software like workflow that integrates synthesis, place and route, and verification into well defined build rule functions that can be easily run, distributed, and cached on multiple machines using the existing capabilities of Bazel.

Today `hdl/bazel_rules_hdl` offers Bazel rules that will synthesize, place and route and run regression tests against the final placed and routed design. The regression tests allow you to set power and area thresholds on subblocks that cannot be exceeded without updating the thresholds, or modifying the problematic RTL.

These build rules give you the ability to setup software like presubmits that prevent RTL modifications that reduce the final PPA of the design, break the place and route or negatively impact synthesis. These types of workflows are common in the software model, but are novel in the hardware workflow space.

The long term goal of this project is that it enables users to run `bazel test //mychip/...` and `bazel build //mychip:gds` and in 10 minutes you have verified and emitted a fabricatable IC even for the most complex designs.

***Index Terms*—hardware tool chain, WOSET 2021, hardware workflows, bazel, software workflows, OpenROAD**

References

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