OpenCache: An Open-Source OpenRAM Based Cache Generator

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What is OpenCache?

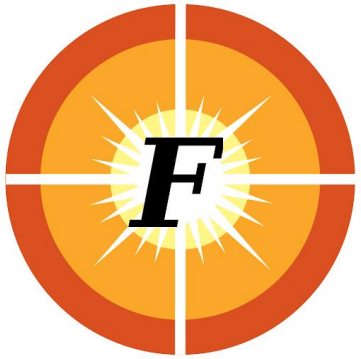
- A custom cache generator
- Open-source software
- Written in Python 3.6
- Built on top of OpenRAM

Why OpenCache?

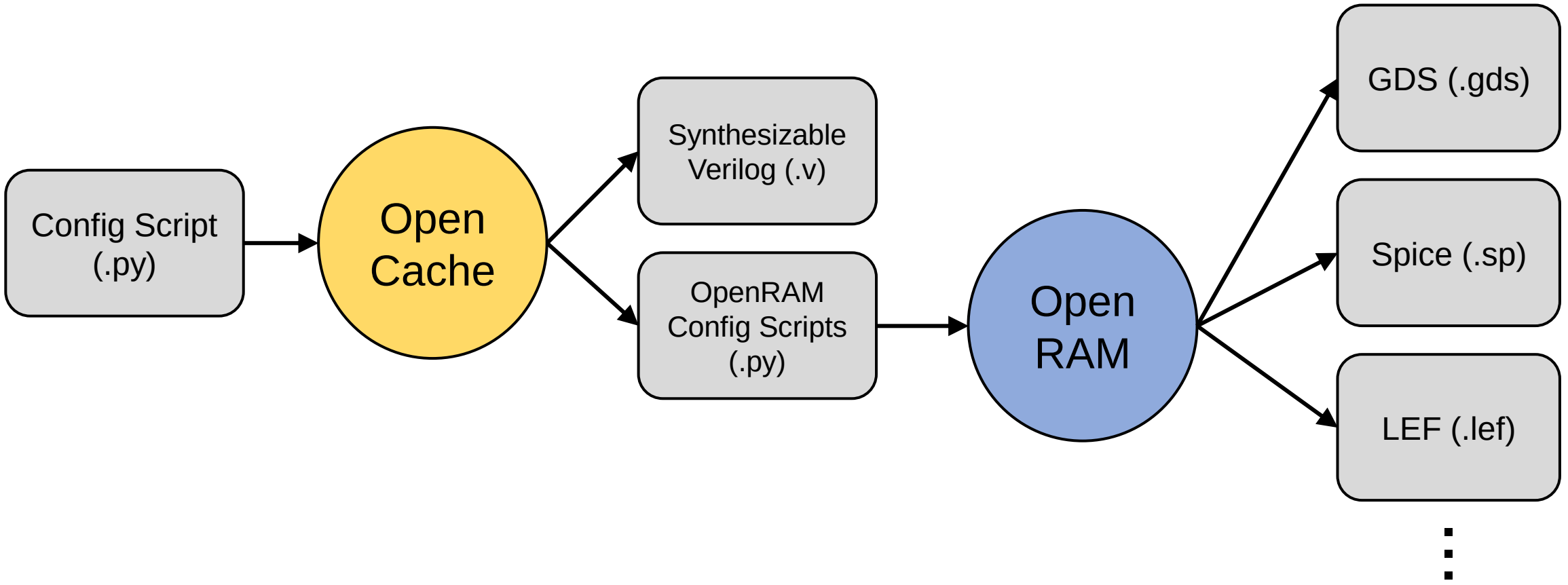
- No other free and open-source custom cache generators
  - Some chip generators have built-in cache generators
- Caches are important for CPU performance
- Ease of designing custom caches
- Efficient memory design, thanks to OpenRAM

Dependencies

- Python 3.6+
- OpenRAM 1.1.17 (or later)
- nMigen 0.2 (or later)
- Verification
  - FuseSoC 1.12 (or later)
  - Yosys 0.9 (or later)
  - Icarus Verilog 10.3 (or later)



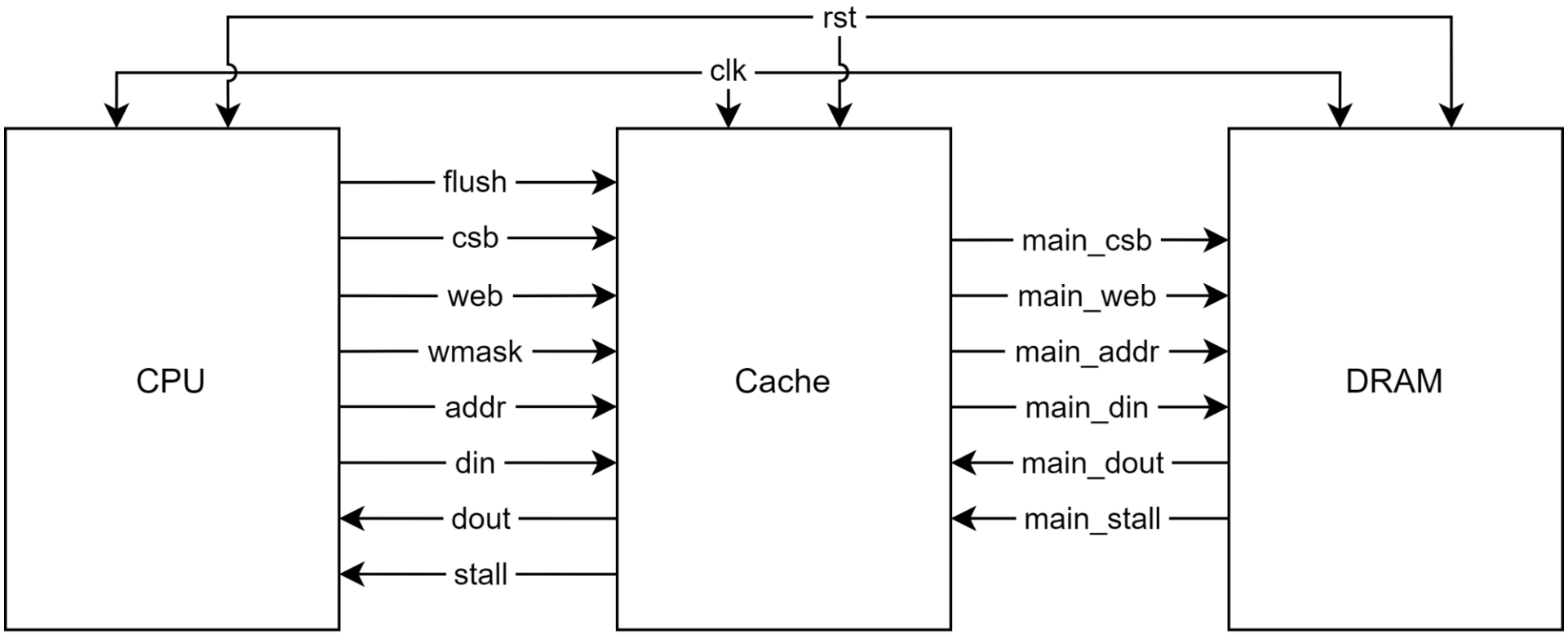
How does it work?



Options

- Memory options
  - Total size
  - Address size
  - Word size
  - Words per line
  - Write size
  - Data hazard
- Cache type
  - Instruction **(WIP)**
  - Data
- Associativities
  - Direct-mapped
  - N-way Set Associative
- Replacement policies
  - First In First Out (FIFO)
  - Least Recently Used (LRU)
  - Random
- Write policies
  - Write-back
  - Write-through **(WIP)**
- Verification options
  - simulate
  - synthesize

Ports


rst
clk
CPU
flush
csb
web
wmask
addr
din
dout
stall
Cache
main_csb
main_web
main_addr
main_din
main_dout
main_stall
DRAM

Conclusion

- github.com/VLSIDA/OpenCache
- Still under development
- Implement missing features
  - Write-through, instruction cache
  - Multi-level cache
  - Multi-port, out-of-order
- More replacement policies (?)
  - PLRU, LIFO, LFU, Clock-Pro, etc.

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