

# From Chisel to Chips in Fully Open-Source



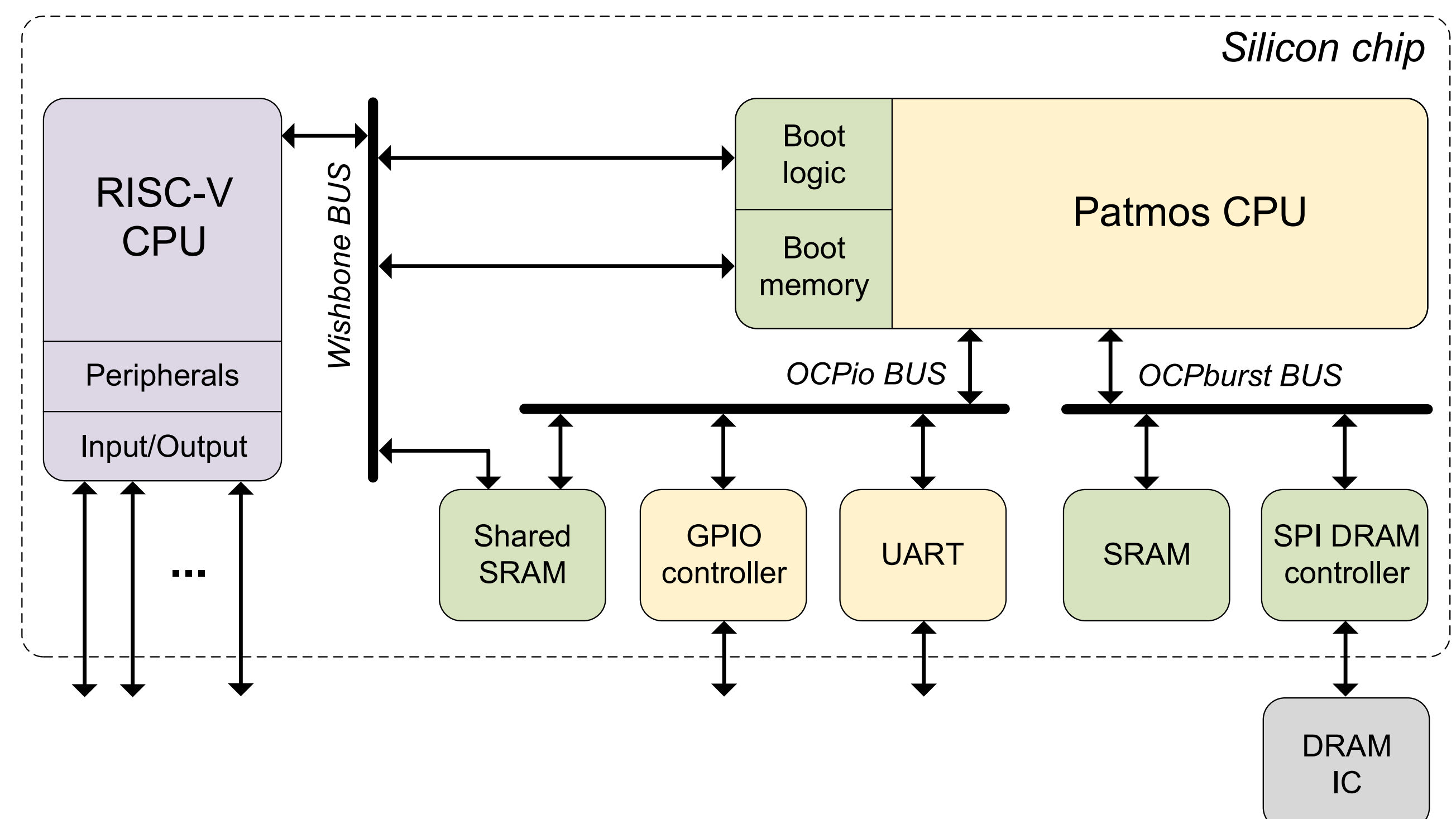
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## Open Source in Software and Hardware

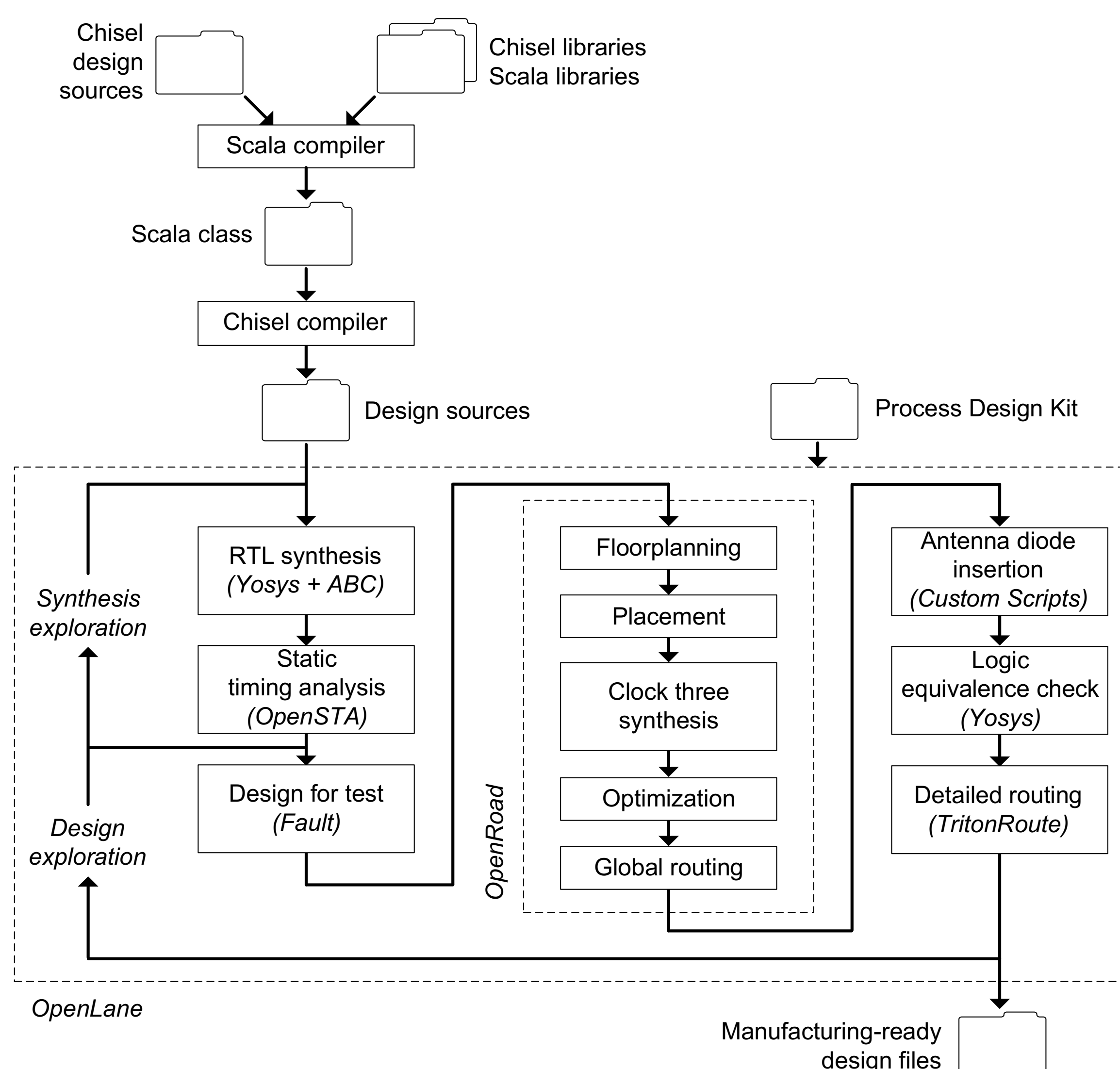
- Open-source software is a success story
  - UC Berkeley's TCP/IP stack powers the Internet
  - Gcc is used to compile Linux
  - Linux runs the servers for the Internet
    - Mobile phones run with Linux
    - Linux is used in embedded devices
  - Apache serves the web pages
  - Java and the JVM run the cloud apps
  - We can browse the Internet with OS Firefox
  - Most languages have an open-source compiler
- OS Hardware is a bit behind
  - Some processor implementations are available
    - Eg., Rocket, Patmos, and some more
  - Tools (simulators, synthesis) are mostly closed source
  - With a few exceptions
    - Chisel as HW construction language
    - Verilator for simulation
    - Yosys and ABC for synthesis

## The Patmos Chip

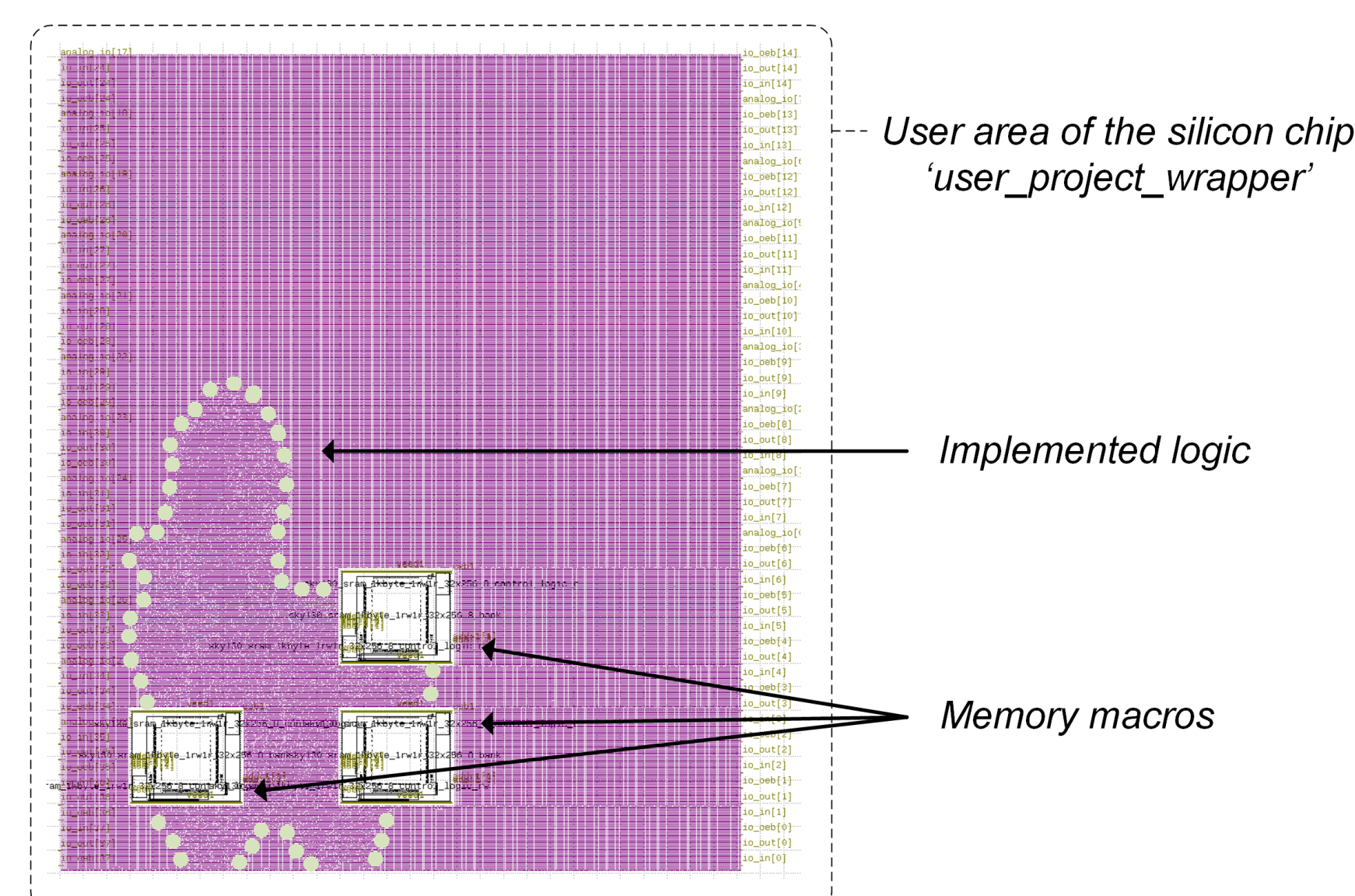


- RISC-V from the Caravel project
- Patmos, GPIO, UART from the Patmos project
- New designs:
  - Boot logic, programmable from the RISC-V core
  - Shared SRAM
  - SPI based memory controller

## OpenLane Tool Flow in a one Semester Course



## Lessons Learned



- We missed MPW 6 by a few hours
  - We did submit for MPW 7
- A chip is doable within one semester
  - With 4th semester students
- It is not as simple as FPGA synthesis
  - No "Play" button
- We should have run the hardening and precheck earlier
- Memories are a pain
- Installation was not so easy
  - Needed some help from a Slack channel
- The open-source move approaches hardware
- Complete flow from Chisel to chips is possible
  - Sponsored by Google
  - Produced by SkyWater on a MPW
- We managed to finish one chip in a semester
  - with 4th semester students
- It was quite fun to do it
- Getting a real chip was a strong motivation for the students