Accelerate Silicon Research with Jupyter Notebooks

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Abstract—In this Work in Progress session we showcase our recent work to leverage Jupyter Notebooks and Conda packages to publish and share interactive silicon design experiments.

Notebooks published at github.com/chipsalliance/silicon-notebooks demonstrate how run a design experiment from design to gds using publicly-hosted notebooks without having to install any tool locally.

Additionally we show how those notebooks can be scaled on a public cloud provider to explore the parameters space of various silicon designs:

- We deploy an open source terraform solution published at github.com/proppy/rad-lab to provision jupyter notebooks with all the necessary tools pre-installed to model our experiments w/ design and flow parameters.
- Between each batch of experiments we report estimated performance metrics to a blackbox and hyperparameter optimization service (which has also an open source im plementation github.com/google/vizier) allowing it to suggest new parameters for future batches.
- We observe that the experiments quickly converge toward the best metrics for the given designs.
- Each of the jobs result in a standalone notebook allowing us to share, aggregate and reproduce every experiments.

Index Terms—silicon, notebook, eda, opensource

Routing

- Input: Technology mapped netlist (Verilog), Physical layout with component cells placed (DEF)
- Output: Physical layout with component cells fully-connected (DEF)
- Metrics: Routing congestion, timing closure estimate

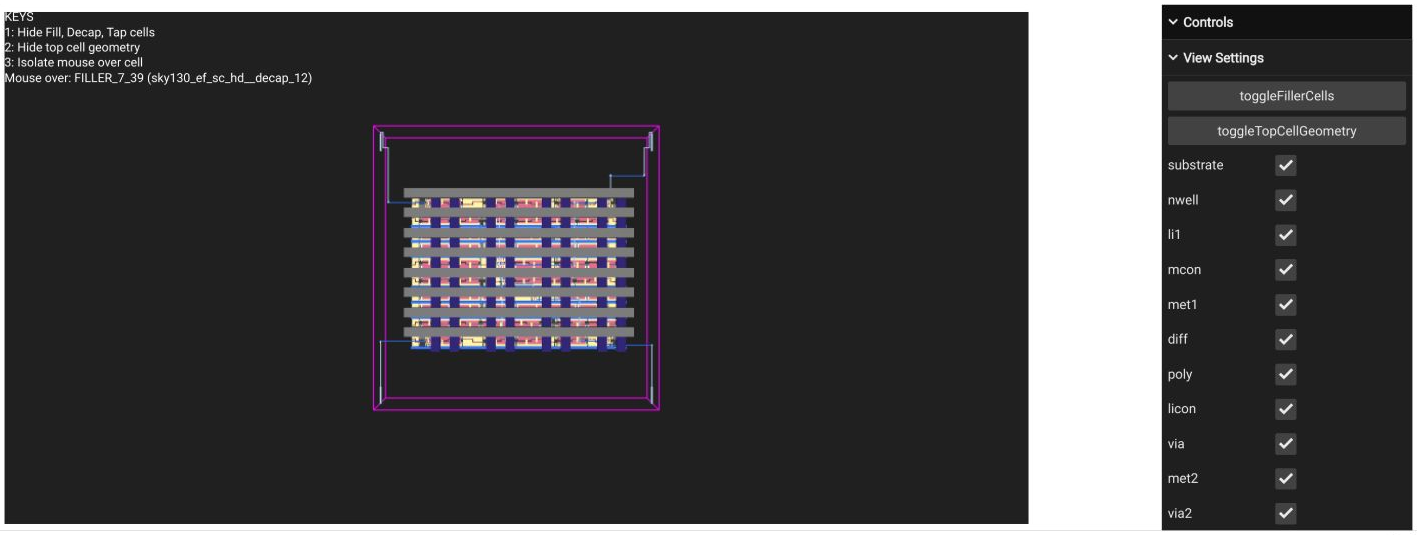
Documentation

```
[ ] !flow.tcl -design . -to routing
```

```
[INFO]: Preparing LEF files for the min corner...
[INFO]: Preparing LEF files for the max corner...
[STEP 1]
[INFO]: Running Synthesis (log: runs/RUN_2022.09.30_11.18.24/logs/synthesis/1-synthesis.log)...
[STEP 2]
[INFO]: Running Single-Corner Static Timing Analysis (log: runs/RUN_2022.09.30_11.18.24/logs/synthesis/2-sta.log)...
[STEP 3]
[INFO]: Running Initial Floorplanning (log: runs/RUN_2022.09.30_11.18.24/logs/floorplan/3-initial_fp.log)...
[WARNING]: Current core area is too small for a power grid. The power grid will be minimized.
[INFO]: Extracting core dimensions...
[INFO]: Set CORE_WIDTH to 38.64, CORE_HEIGHT to 27.2.
[STEP 4]
[INFO]: Running IO Placement...
[STEP 5]
[INFO]: Running Tap/Decap Insertion (log: runs/RUN_2022.09.30_11.18.24/logs/floorplan/5-tap.log)...
[INFO]: Power planning with power {VPWR} and ground {VGND}...
[STEP 6]
[INFO]: Generating PDN (log: runs/RUN_2022.09.30_11.18.24/logs/floorplan/6-pdn.log)...
[STEP 7]
[INFO]: Running Global Placement (log: runs/RUN_2022.09.30_11.18.24/logs/placement/7-global.log)...
[STEP 8]
[INFO]: Running Placement Resizer Design Optimizations (log: runs/RUN_2022.09.30_11.18.24/logs/placement/8-resizer.log)...
[STEP 9]
[INFO]: Removing Buffers from Nets (If Applicable) (log: runs/RUN_2022.09.30_11.18.24/logs/placement/9-remove_buffers.log)...
[STEP 10]
[INFO]: Running Detailed Placement (log: runs/RUN_2022.09.30_11.18.24/logs/placement/10-detailed.log)...
[STEP 11]
[INFO]: Running Placement Resizer Timing Optimizations (log: runs/RUN_2022.09.30_11.18.24/logs/cts/11-resizer.log)...
[STEP 12]
[INFO]: Removing Buffers from Nets (If Applicable) (log: runs/RUN_2022.09.30_11.18.24/logs/placement/12-remove_buffers.log)...
[STEP 13]
[INFO]: Running Global Routing Resizer Timing Optimizations (log: runs/RUN_2022.09.30_11.18.24/logs/routing/13-resizer.log)...
[STEP 14]
[INFO]: Removing Buffers from Nets (If Applicable) (log: runs/RUN_2022.09.30_11.18.24/logs/placement/14-remove_buffers.log)...
[STEP 15]
[INFO]: Running Detailed Placement (log: runs/RUN_2022.09.30_11.18.24/logs/routing/15-diode_legalization.log)...
[STEP 16]
[INFO]: Running Global Routing (log: runs/RUN_2022.09.30_11.18.24/logs/routing/16-global.log)...
[INFO]: Starting OpenROAD Antenna Repair Iterations...
[STEP 17]
[INFO]: Writing Verilog (log: runs/RUN_2022.09.30_11.18.24/logs/routing/16-global_write_netlist.log)...
[STEP 18]
[INFO]: Running Fill Insertion (log: runs/RUN_2022.09.30_11.18.24/logs/routing/18-fill.log)...
[STEP 19]
[INFO]: Running Detailed Routing (log: runs/RUN_2022.09.30_11.18.24/logs/routing/19-detailed.log)...
[INFO]: No DRC violations after detailed routing.
[INFO]: Saving current set of views in 'runs/RUN_2022.09.30_11.18.24/results/final'...
[INFO]: Saving runtime environment...
[INFO]: Generating final set of reports...
[INFO]: Created manufacturability report at 'runs/RUN_2022.09.30_11.18.24/reports/manufacturability.rpt'.
[INFO]: Created metrics report at 'runs/RUN_2022.09.30_11.18.24/reports/metrics.csv'.
[INFO]: There are no max slew, max fanout or max capacitance violations in the design at the typical corner.
[INFO]: There are no hold violations in the design at the typical corner.
[INFO]: There are no setup violations in the design at the typical corner.
[SUCCESS]: Flow complete.
[INFO]: Note that the following warnings have been generated:
[WARNING]: Current core area is too small for a power grid. The power grid will be minimized.
```

Preview

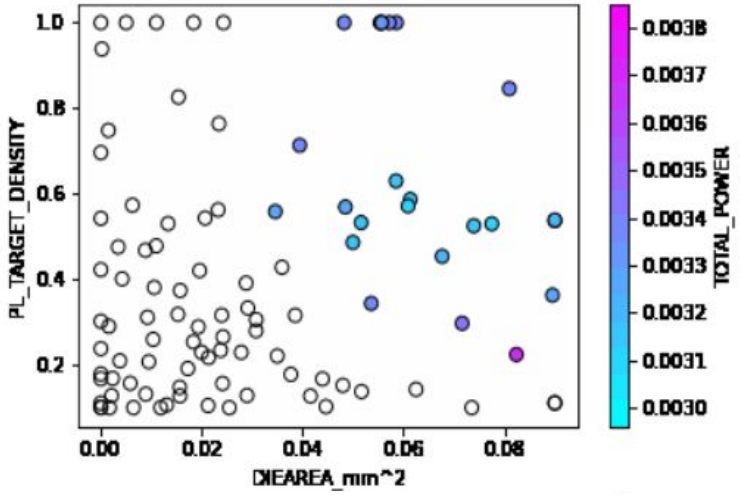
Show code

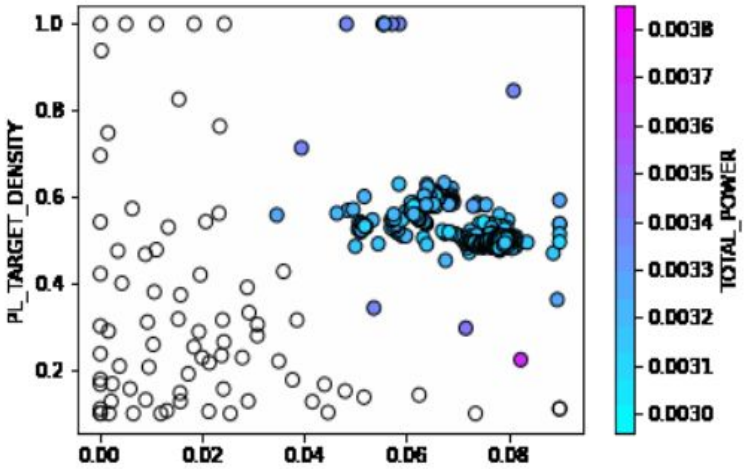


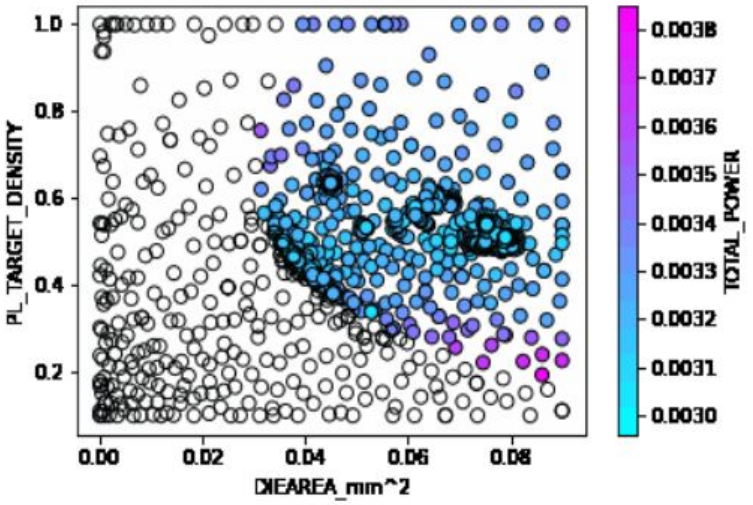
Explore design parameters space

with Cloud-based hyper-parameters tuning

Find best design parameters to **minimize power consumption**

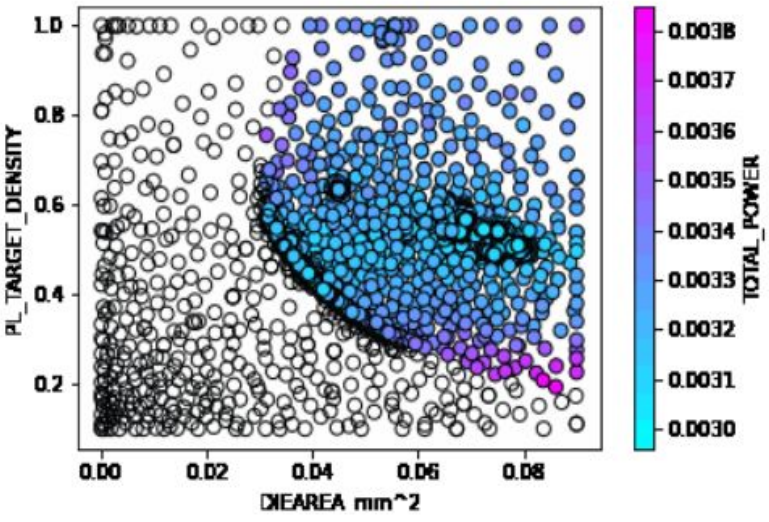






[196]:

area	density	ppa
0.0019	75.00%	0.00000098
0.0025	60.00%	0.00000120
0.0025	60.00%	0.00000101
0.0100	40.00%	0.00000144
0.0400	20.00%	0.00000174
0.0064	50.00%	0.00000121
0.0064	90.00%	0.00000116
0.0064	70.00%	0.00000121
0.0064	70.00%	0.00000116
0.0064	80.00%	0.00000129
0.0064	40.00%	0.00000115
0.0064	50.00%	0.00000109
0.0064	60.00%	0.00000132
0.0064	70.00%	0.00000129
0.0064	80.00%	0.00000132
0.0064	40.00%	0.00000129
0.0064	50.00%	0.00000130
0.0064	20.00%	0.00000114
0.0064	40.00%	0.00000130



Find best pipeline stages to **maximize slack**