BITSTREAM CHEF

WOSET-2022

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Introduction

- Electronic Design Automation (EDA) technologies have become increasingly important in their fields of application with the open-source revolution in the silicon industry.

- These tools cover a wide range of automatic operations that save a significant amount of time.

- Bitstream Chef targets domains of both ASIC and FPGA flow.

- In FPGA flow it generates the bitstream of a design by taking an RTL design, allowing the user to map I/Os onto an FPGA using a GUI, and thus generating the bitstream through automated processes by use of an open-source tool F4PGA.

Introduction (cont.)

- Additionally, it uploads the Bitstream onto the connected FPGA board while also letting the user know whether any boards are currently connected.

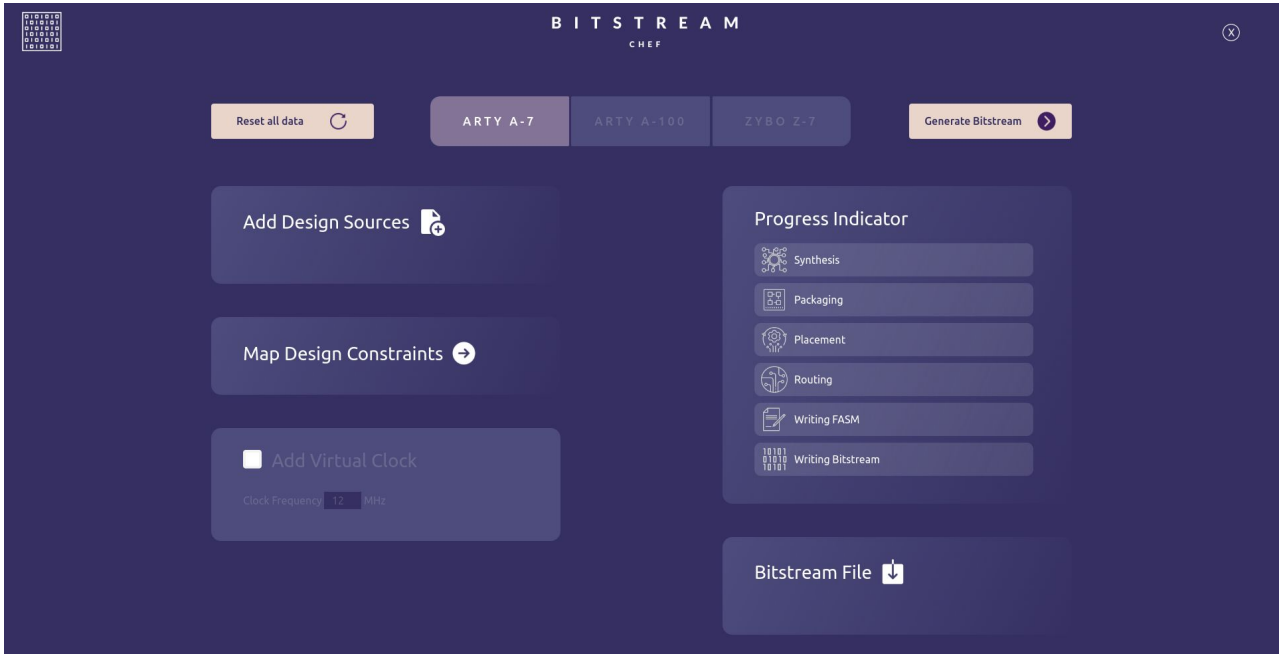
- It will also allow user to either have pre-defined program embedded in the bitstream or upload the program separately through UART.

- In ASIC flow of Chef the selected RTL design move towards the GDS generation step.

- It has the Open Lane toolchain integrated for ASIC flow. Bitstream Chef is designed to be the go-to tool for every developer who frequently must upload or burn designs into FPGA, has a computer with less computing power.

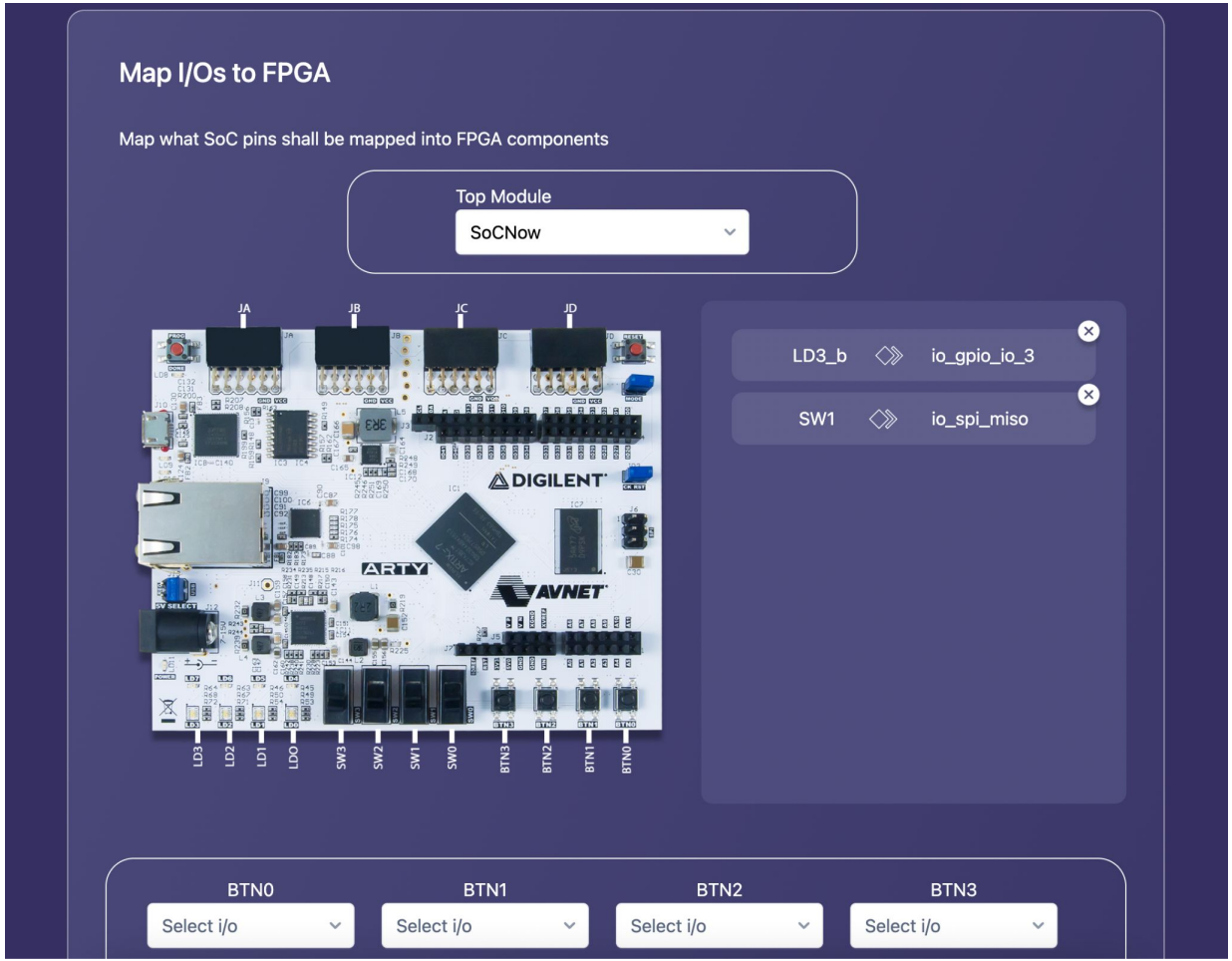
Flow

User can add their design sources in Bitstream Chef by pressing the `Add Design Sources`



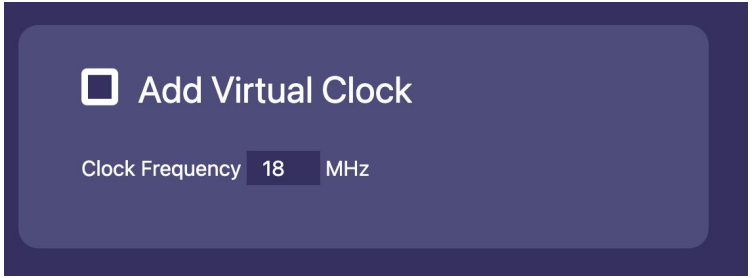
Flow (cont.)

Map the input and outputs of your design on FPGA using GUI mapper.

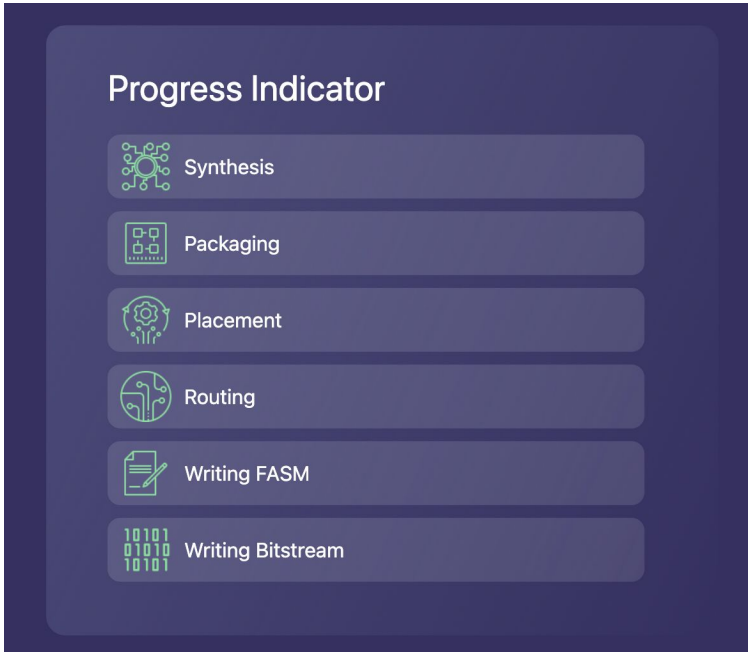


Flow (cont.)

Add Virtual Clock



Progress Indicator



Tools Used

- F4PGA
  - Yosys
  - NextPnR
- Python
  - EEL
- Electron JS

Solution to the Problem

- In the scenario of using open source tools for Bitstream Generation, their is so much work to do manually by the user.
- Bitstream Chef resolves this issue by providing a one screen GUI, for the entire bitstream generation.
- It is built on top of F4PGA toolchain, that works as a wrapper for Yosys, AutoPnR and other bitstream generation process tools.

Applications

- Quick Bitstream Generation
- Easy and automated Constraint file creation.
- Detecting and Uploading bitstream onto the FPGA (Not implemented yet)
- Live Program burning onto the FPGA (Not implemented yet)
- User can also check all the process steps outputs like synthesis (Not implemented yet)
- Quick GDS Generation by use of OpenLane (Future Work)

Demonstration

Contributors

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Acknowledgement

- We would like to acknowledge Micro Electronics Research Lab for providing us with required training and letting us capable of using state of the art technologies.
- We would also like to acknowledge open source tools such as F4PGA, Yosys, AutoPnR.