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Generate Custom SoC

User can generate custom SoC by providing configurations for Core RV32(i,m,f,c), devices (gpio, spi, spi-flash, uart, i2c, timer) and Bus interconnects (wishbone, tl-ul, tl-c).

Generate Bitstream

User can generate bitstream of the generated SoC by providing the SoC I/O Mapping onto FPGA Components and writing a program to be run on top of burned bitstream

Generate Reusable SoC Component

User can generate any single verified reusable SoC Component including, any core combination, any device and/or any single bus interconnect

Generate Verification Report

User can generate verification report by selecting the compliance tests from the provided list. The report will contain either the selected tests passed or failed.

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