Baskin Engineering UC SANTA CRUZ

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Google Summer of Code

OpenRegFile

Open Source Register File Generation

Mentee: Talha Ahmed, **Mentor**: Mathew R. Guthaus, Jesse Cirimelli-Low

Introduction:

This work presents an extension of the OpenRAM memory compiler to provide the automated generation of latch-based register files. It uses standard cells from the Skywater 130nm library. OpenRegFile automatically generates a spice netlist, layout, and a verilog model. It leverages the hierarchical decoders and muxes from SRAM designs. The cells for the decoders and muxes in SRAMs are custom made but we replace them with standard cells to improve routability and portability to other technologies with a cell library. At first, we created a register file array along with a tristate. The tristate helps to use the same data-line throughout the array of D-Latches which improves routing. We used the spice netlist API to implement the logic in OpenRAM and created custom modules to create the layout.

Details:

Fig. A: Generated latch array 5 rows, and 3 columns, with tristate and well taps(to prevent latch-up issue) for every two latches in a row.

Fig. B: 2x4 Decoder using standard cells of AND and INV.

Fig. C: Logic circuit of 2W1R 4x5 register file is implemented in Logisim for better understanding the structure for implementation in OpenRAM. It uses the same data line by using the tristate for better routing. Main-subsdiary latch architecture is used to prevent race-around condition.

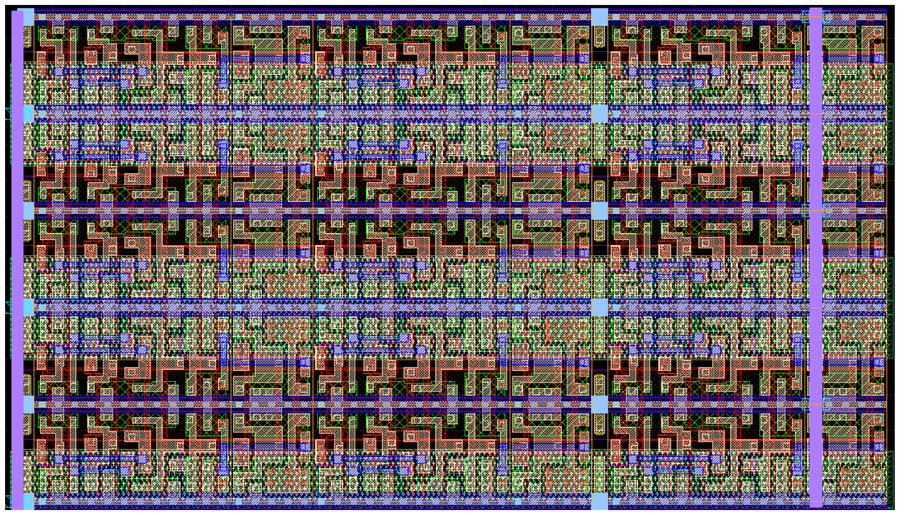

Fig. A

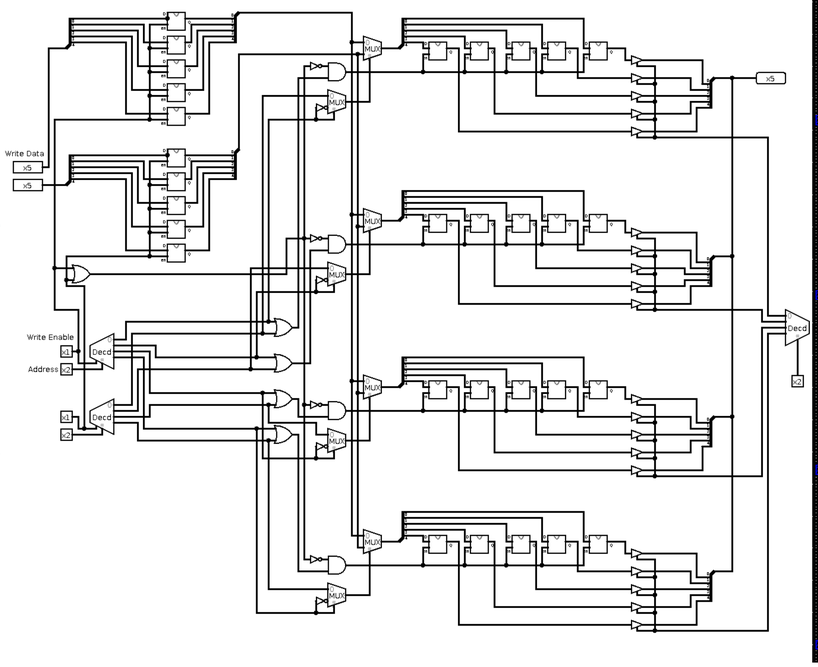

Fig. C

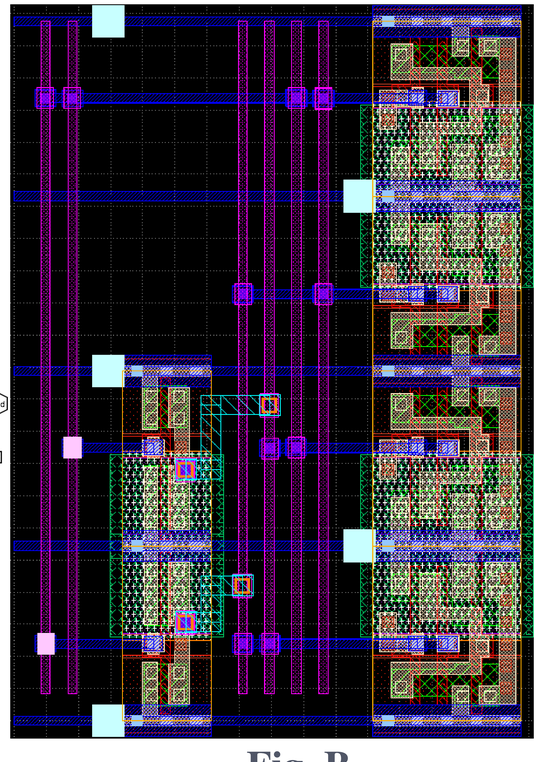

Fig. B