An RFIC-oriented flow for Planar Inductors modeling and generation aiming Open-Source PDKs

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***Abstract*—This paper presents an RFIC-oriented flow that aims to provide a way to modeling and generation of inductors based on open-source PDKs. A proposed flow is presented in order to be part of an RFIC design flow compatible with mainstream Analog open source development. An LC filter example using skywater 130 nanometer open-PDK is provided to show the proposed flow and its integration with other open-source tools that aim to obtain a final verified RFIC layout.**

I. Introduction

Recent progress in open-source silicon reflects the need for democratization of the IC Design process in the semiconductor industry [1]. This can help fill some gaps that were cited as an alert on recent global chip shortage [2] and a way to attract new talents [3] . By leveraging collaborative channels in all aspects of IC Design (e.g. tools and PDKs), the community can take the advantages of the open source movement to the way of innovation and costs reduction, acceleration the design-to-production cycle, and providing a real way to IP sharing across industry and academia, fostering a more inclusive and dynamic ecosystem.

Despite the fact that progress can be tracked by these recent developments in open-source IC design, most of the work arrives in digital or analog low-frequency projects, which can also take advantage of the new TinyTapeout approach [4], since the RFIC design does not yet have a consolidated flow. However, RFICs are part of some important applications such as smartphones [5], Internet of Things [6], 5G [7], and quantum computing [8], among others, and deserve to be included in this democratization of the IC design process.

One of the main bottlenecks in RFIC design is the correct modeling of passives such as inductors and its integration with the other circuits in a development flow [9].

In this work, an RFIC-oriented flow is presented for inductors modeling and generation using the ASITIC [10] tool and a way to integrate it into an open source IC design flow. An example of parallel LC filter design using skywater 130 nanometer open PDK [11] is also provided to show the proposed flow in an RFIC development, including physical verification using magic [12] and netgen [13], and simulations using Xschem [14] and ngspice [15].

II. Inductor modeling and proposed flow

The equivalent circuit for the inductor (Fig. 1) [16] incorporates its inherent parasitic elements. The series resistance R represents the resistance of the wire that forms the inductor. The shunt resistances $Rs1$ and $Rs2$ account for the substrate losses. Finally, the shunt capacitances $Cs1$ and $Cs2$ represent the capacitance between the inductor and the substrate. Consequently, this model offers a more accurate representation of the behavior of the integrated inductor.

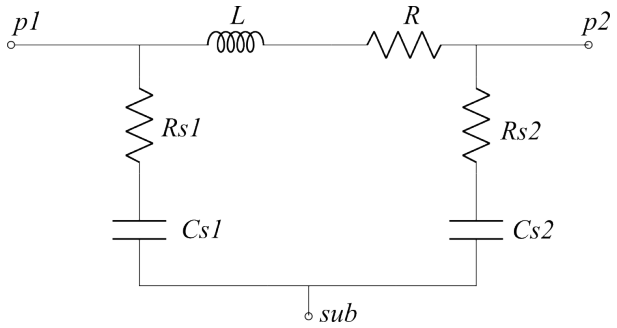

Fig. 1. Pi-equivalent circuit of the inductor. [16]

In order to perform the proper inductor modeling and also to generate this modeled inductor to be used on an integrated circuit development, the flow (Fig. 2) is proposed.

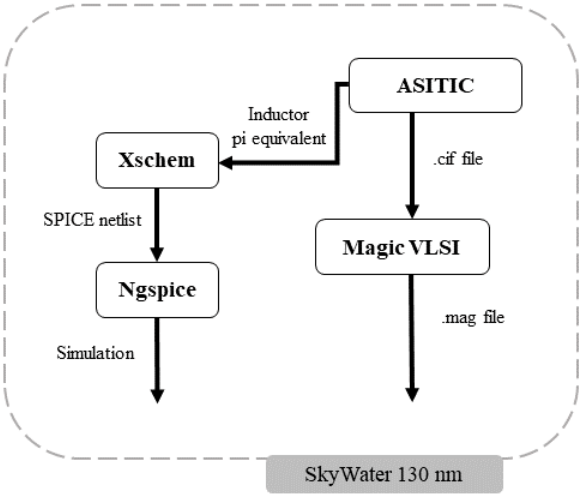

Fig. 2. Proposed inductor modeling flow.

The ASITIC tool, using a pre-made Sky130 PDK technology file, is used to model the inductor. As an application

example, initially the function *optsq* is used to create a *1 nH* square inductor with an optimal *Q* factor (Fig. 3). It occupies an area of 120 μm x 132 μm = 0.016 mm². Subsequently, the function *pix* was utilized at 2.5 GHz to determine the pi-equivalent circuit (Fig. 1) of the inductor, along with its Q factor and self-resonant frequency. Finally, the inductor layout was exported as a CIF (Crystallographic Information Framework) file using the *cifsave* command.

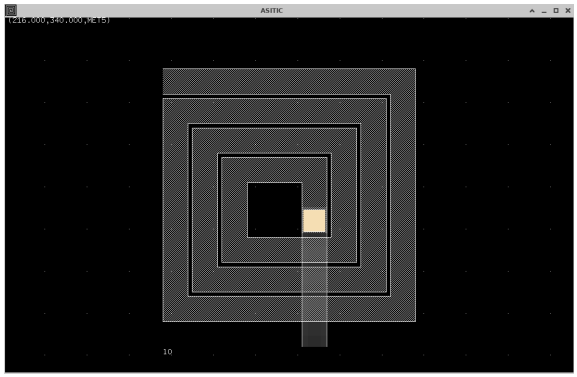

Fig. 3. The 1 nH inductor generated by ASITIC (grid = 20 μm).

Using the pi-equivalent circuit with the Xschem and ngspice tools, it became feasible to simulate its impedance, real part, and imaginary part to verify its self-resonant frequency by using the AC simulation. Moreover, the inductor CIF file can be read by the Magic tool and saved as a *.mag* file. Also, Magic can be used to generate a final GDS (Graphic Design System) file.

III. Inductor Simulation

The Fig. 4 illustrates that the inductor exhibited a maximum *Impedance* and *Real Part*, in addition to a zero *Imaginary Part*, at its self-resonant frequency of 27.58 GHz. This frequency is ten times greater than the ISM 2.5 GHz oscillation frequency, ensuring the inductor's proper operation within this frequency band.

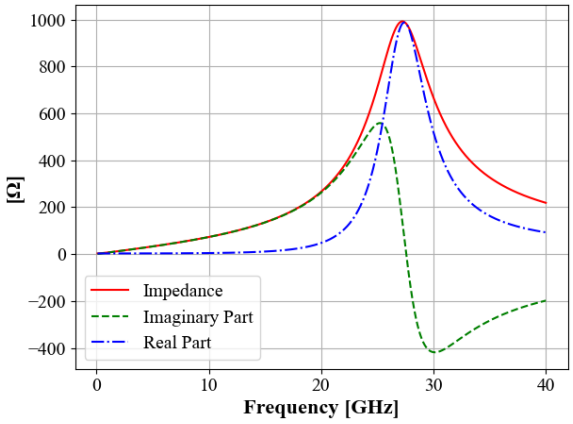

Fig. 4. Inductor's Impedance, Real and Imaginary Part simulation to check it self-ressonant frequency.

Besides determining the self-resonant frequency from the simulation, it is also feasible to extract other parameters, such as the *Q* factor, from the results. Additionally, analyzing these parameters can provide a deeper insight into the performance and efficiency of the inductor in various operating conditions. This information is crucial for optimizing design specifications and improving the overall circuit functionality.

The next section will present the use of this inductor in an LC filter.

IV. LC Filter Design

With the inductor *.mag* and its pi-equivalent circuit provided by the inductor modeling and generation flow, the parallel LC filter (Fig. 5) is used as a circuit example.

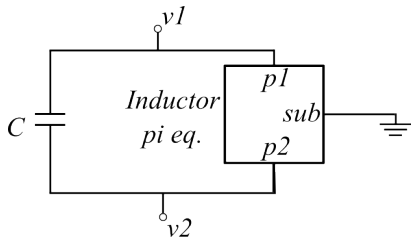

Fig. 5. Parallel LC filter schematic.

In Fig. 5, the inductor is shown as a box with two terminals and a substrate contact that facilitates the comprehension of the pi-equivalent circuit model.

To show its feasibility, Fig. 6 presents its RFIC-oriented design flow proposed for this design.

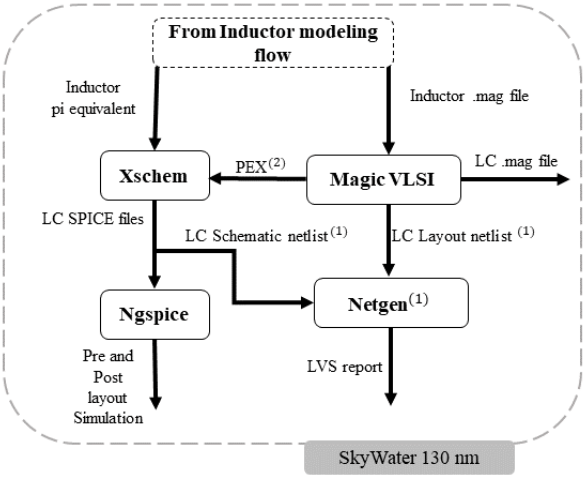

Fig. 6. Flow for the LC circuit design.

This flow is similar to an analog IC design flow, encompassing: pre- and post-layout simulation with Xschem+Ngspice; layout and parasitic extraction (PEX) with Magic; and layout versus schematic (LVS) verification with Netgen. The designed LC circuit occupies an area of 202.06 μ m x 183.05 μ m, which is equal to a total area of 0.037 mm². The layout can be seen on Fig. 7.

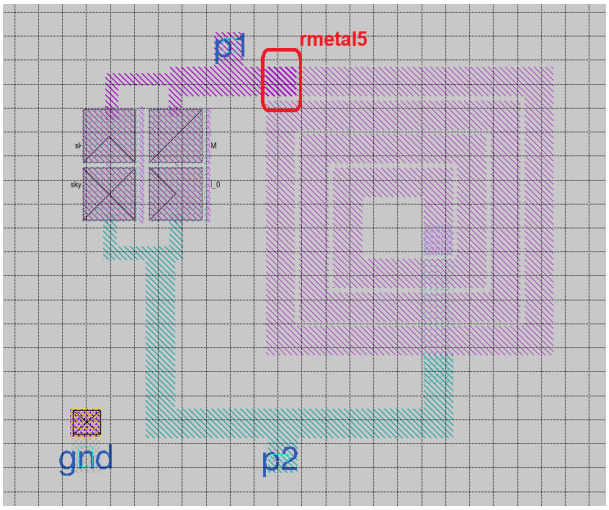

Fig. 7. LC circuit layout (grid = 10 μm).

However, some modifications were implemented to incorporate the inductor into the circuit inside this flow. The first significant modification [1] involved the addition of the *rmetal5* layer to one port of the inductor, which is highlighted in Fig. 7. Although this layer is a metal at the physical level, it is extracted as a resistor during netlist extraction from the Magic VLSI layout tool. This modification prevents short circuits because the inductor is effectively treated as a wire by the tool. Consequently, for LVS purposes, the circuit is considered to consist of capacitor C and a single resistor (*rmetal5*) in place of the inductor, as shown in Fig. 8.

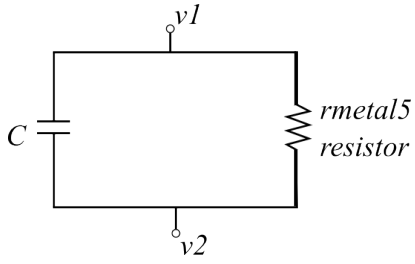

Fig. 8. Parallel LC filter schematic considered to LVS.

The second modification [2] involved removing the inductor from the layout before performing the Post-Extraction (PEX) as illustrated in Figure 9. This step is essential because the inductor's pi-equivalent circuit already includes its intrinsic parasitics.

This means that the PEX process will focus only on extracting the remaining parasitics from the overall LC circuit. By excluding the inductor during PEX, we ensure that the resulting parasitic extraction is accurate and does not double-count the inductor's inherent parasitics. Consequently, this approach allows for more precise post-layout simulations, as the extracted parasitics can be combined with the pre-existing inductor model, leading to a comprehensive and accurate simulation of the LC circuit's behavior.

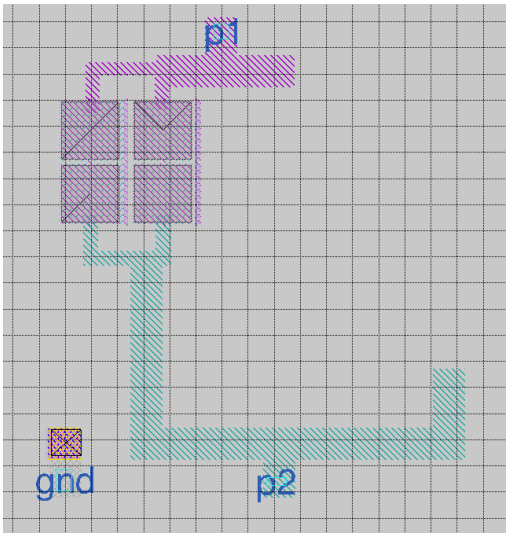

Fig. 9. Parallel LC filter layout considered to PEX (grid = 10 μm).

Through AC simulation with Xschem+Ngspice, the *Impedance*, *Real Part* and *Imaginary Part* of the LC circuit were analyzed for both pre- and post-layout (Fig. 10). The LC circuit reached its maximum post-layout *Impedance* at a frequency of 2.45 GHz. In particular, a frequency shift of around 50 MHz occurred when the parasitic extraction (PEX) data was incorporated into the simulation, accompanied by changes in the magnitudes of these parameters.

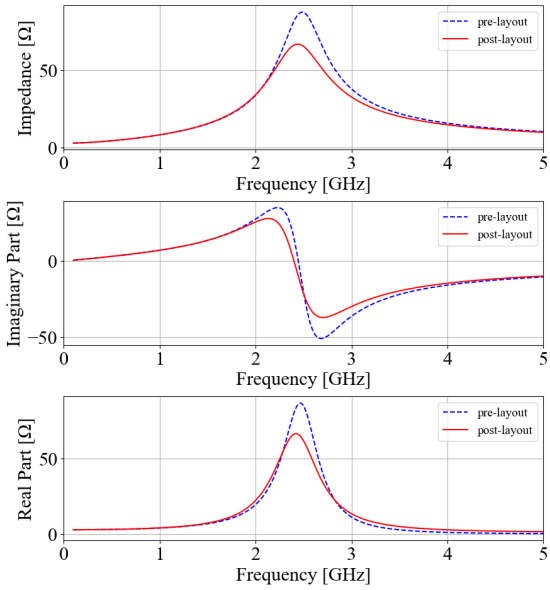

Fig. 10. LC's Impedance, Real and Imaginary Part simulation pre- and post-layout.

All the source files and a description of how to perform the flow steps can be found in a github repository [17].

V. Conclusions and Future Works

This paper shown the design of an LC circuit in order to demonstrate the feasibility of a proposed inductor modeling and generation flow that can be incorporated in a open source IC design flow aimed for RF circuits.

The proposed flow uses popular open source tools on Analog IC Design together with ASITIC and some proposed modifications to do an RFIC-oriented design.

The development of an open source alternative to ASITIC, which is a freeware, and the use of EM solvers inside the design tools are future works needed to improve this flow, as well as the support to other open PDKs and a way to provide indirect testing using TinyTapeouts.

Although RFIC designs require more than just inductor synthesis, this step plays a crucial role in developing a more comprehensive RF Open Source IC (RFOSIC) Design Flow.

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