

OpenROAD Update

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WOSET
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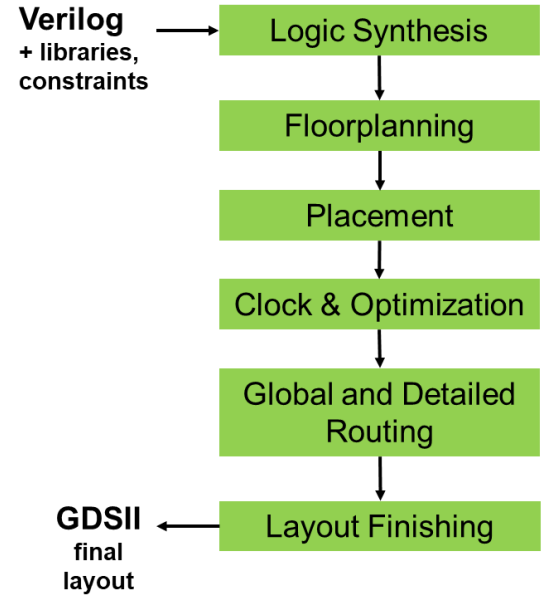
precision



PII products based on OpenROAD provide Application Specific Integrated Circuit (ASIC) and System on Chip (SoC) design teams with an open source, no-human-in-loop, 24-hour place and route solution. It was initially developed with funding from DARPA under the Intelligent Design of Electronic Assets (IDEA) program. Precision Innovations is the primary industry developer and is commercializing this technology.

OpenROAD: No Humans, 24 Hours

- Directly attack the crises of design and innovation
 - **Schedule** barrier: **RTL-to-GDS** in 24 hours
 - **Expertise** barrier: No-human-in-loop, tapeout GDS
 - **Cost** barrier: Open source (and, runs in 24 hours)
 - **Accessibility** barrier
- FOCUS: Ease of use and runtime
 - Freedom from choice
- Unleash system innovation and design innovation
- Enable tool customization to system, application needs
- **Foundation for hardware innovation, research, education, workforce development**

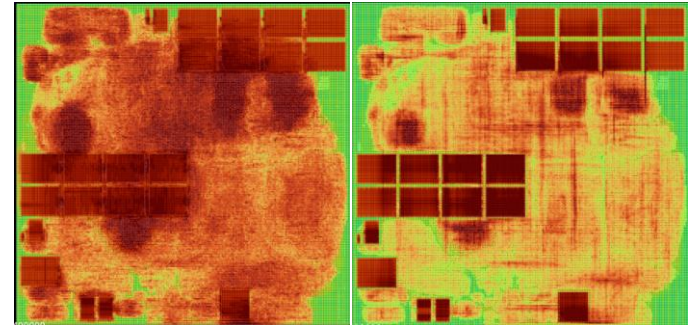
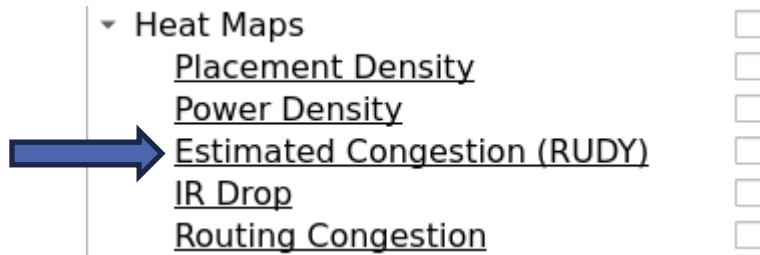


Engagement

- Merging 100-200 Pull Requests per month in GitHub
- 124 Contributors to OpenROAD ; 72 contributors to OpenROAD-flow-scripts
- Completed all work for the original DARPA grant
- Joining the Next Generation Microelectronics Manufacturing (NGMM) Program at Texas Institute for Electronics (TIE) at The University of Texas at Austin. The focus will be supporting 3D Heterogenous Integration (3DHI) in OpenROAD
- OpenROAD is being used in India for large scale training, lead by IITG (Guwahati). >2,800 students expected

Placement

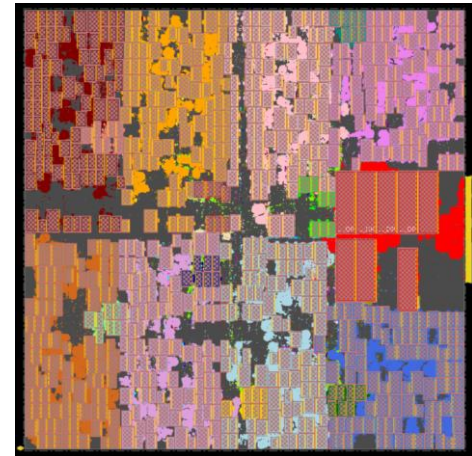
- Global placement
 - RUDY – a faster congestion estimation
 - Available in the GUI



Global Route

RUDY

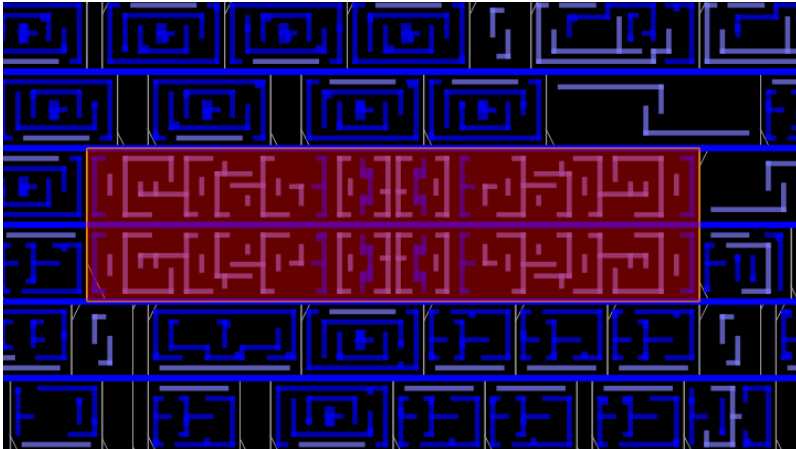
- Hierarchical RTL-MP replaces TritonMacroPlacer



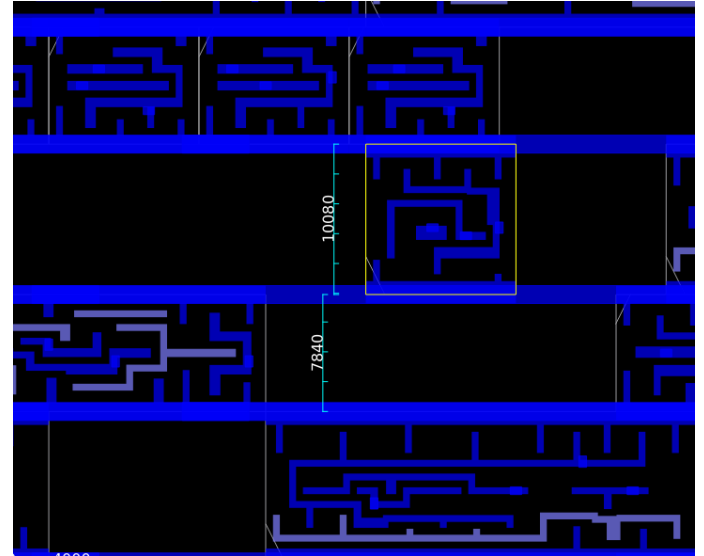
Placement

- IO Pin Placement
 - Constraints – regions, keep-out, mirrored pins
 - Annealing – for larger problems

Multi-Bit Flip-Flop (MBFF) Clustering



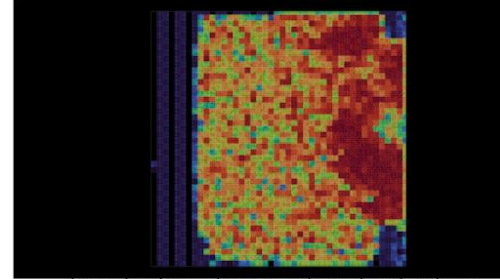
Hybrid (Non-Uniform) Rows



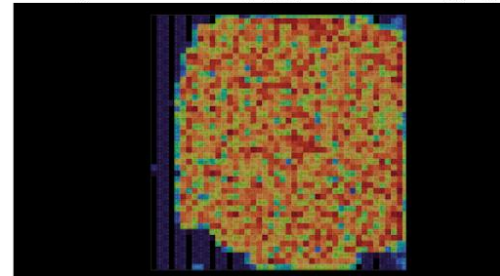
Optimization

- Repair_design inside of global placement
 - Previously we did repair after global placement which can lead to hotspots
 - Further work will look repair_timing as well
- Timing repair
 - Previously only done during post-CTS and extra margin had to be applied to account for routing
 - Post global routing – incremental global routing with RC estimation
 - Post detailed routing – incremental detailed routing with incremental signoff RCX

sky130ns-riscv32i-stg3_5_place_dp-Pdensity.png

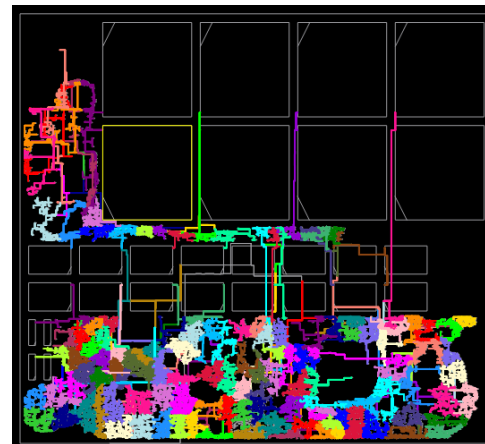
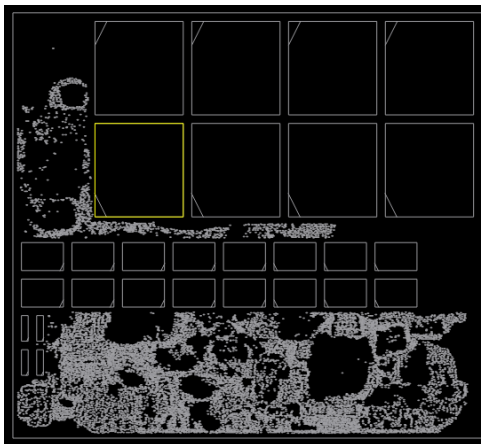
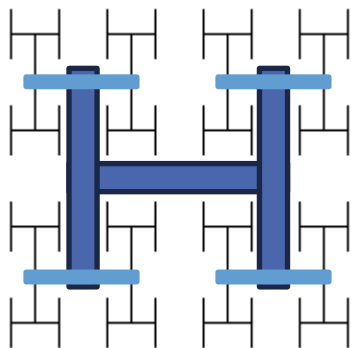


sky130hs-riscv32i-stg3_5_place_dp-Pdensity.png



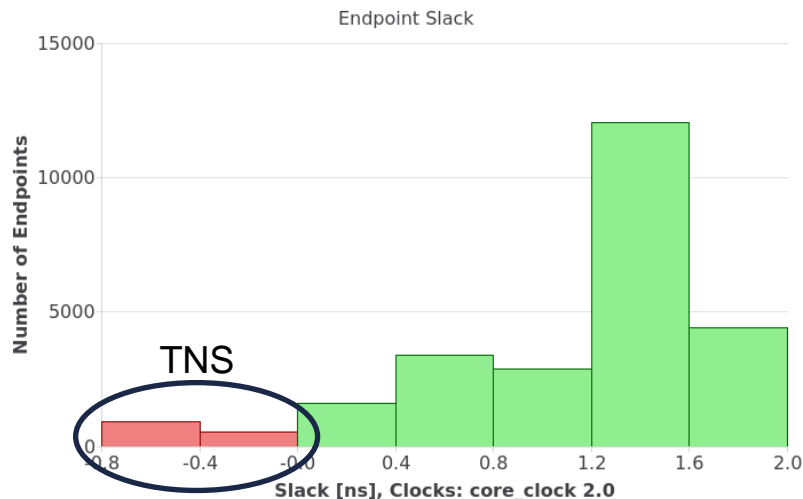
Optimization (2)

- Clock-Tree Synthesis (CTS)
 - Obstruction aware – morph the H-tree to avoid obstructions
 - Dummy loads – add extra loads to balance the clock tree
 - NDR – apply non-default routing rules to clock nets
 - Clock gating – better balancing of the tree across clock gates



Optimization (3)

- Resizer
 - New transforms: buffer removal, gate cloning, pin swapping
 - Gain based buffering– pre-placement buffering algorithm based on abc
 - Dead logic elimination – yosys doesn't do cross boundary optimization with hierarchy
- Optimize total negative slack (tns) beyond the worst slack (wns)



Operator Mapping

- We need to select an implementation for each operator
- At synthesis time we have limited information about timing, so we don't want to make a hard choice
- Allow operator implementations to be swapped in OpenROAD to improve performance or save area/power

Public library of arithmetic operators from ETH Zurich at <https://github.com/pulp-platform/ELAU>

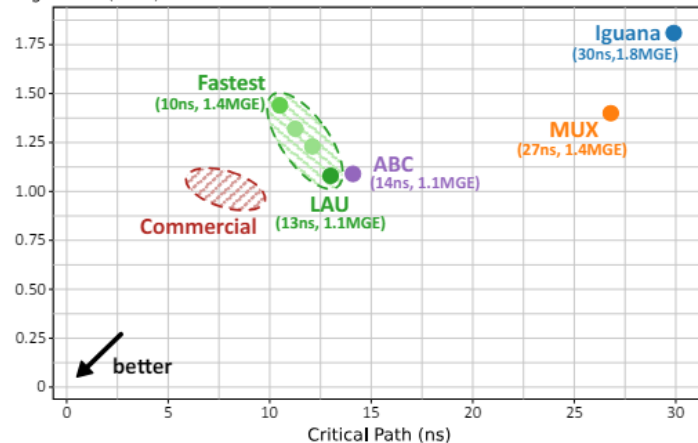
Verilog:

```
assign o1 = a1 * b1;  
assign o2 = a2 * b2;
```

Small
Slow

Big
Fast

Logic Area (MGE)



Courtesy ETH Zurich

Odds and Ends

- openroad -python
 - Design, Tech, and Timing APIs
 - No GUI (yet)
- Antenna checking rewritten with multi-threading. Incremental repair and wire jumpers improve convergence and reduce diodes.
- GF12: routing improvements (additional rules)
- GUI: slack histogram performance improvements for path groups.
- ORAssistant