WOSET 2018 Agenda

8:00 - 8:30 Morning Coffee Break (beverages only)

Introduction (8:30am - 9:10 am)
8:30 am - 8:35 am. Opening statement (Sherief Reda)
8:35 am - 8:50 am. Andreas Olofsson (DARPA)
8:50 am - 9:00 am. State of the digital flow (A. B. Kahng)
9:00 am - 9:10 am. State of the analog flow (S. Sapatnekar)

Session 1: Infrastructure, Interfaces and Standards (9:10 - 09:40)
Session chair: Sherief Reda, Brown University

09:10 - 09:20: LGraph: A multilanguage open-source database.
Rafael Trapani Possignolo, Sheng Hong Wang, Haven Skinner and Jose Renau

09:20 - 09:30: OpenPiton: An Emerging Standard for Open-Source EDA Tool Development
Jonathan Balkind, Alexey Lavrov, Michael McKeown, Yaosheng Fu, Tri Nguyen, Mohammad Shahrad, Ang Li, Katie Lim, Yanqi Zhou, Ting-Jung Chang, Paul Jackson, Adi Fuchs, Samuel Payne, Xiaohua Liang, Matthew Matl and David Wentzlaff

09:30 - 09:40: Cpp-Taskflow: Fast Parallel Programming with Task Dependency Graphs
Chun-Xun Lin, Tsung-Wei Huang, Guannan Guo and Martin Wong

9:40 - 10:15 First poster session (all papers)
Mid-morning Coffee Break (beverages only)

Session 2: Almost-full flow tools and Infrastructure (10:15 - 10:45)
Session chair: Mohamed Shalan, American University in Cairo (AUC)

10:15 - 10:25: DATC RDF: An Open Design Flow from Logic Synthesis to Detailed Routing
Jinwook Jung, Iris Hui-Ru Jiang, Jianli Chen, Shih-Ting Lin, Yih-Lang Li, Victor N. Kravets and Gi-Joon Nam

10:25 - 10:35: Rsyn - A Physical Synthesis Framework for Research and Education
Mateus Fogaça, Jucemar Monteiro, Marcelo Johann and Ricardo Reis

10:35 - 10:45: Parallel Tools for Asynchronous VLSI Systems
Yi-Shan Lu, Samira Ataei, Jiayuan He, Wenmian Hua, Sepideh Maleki, Yihang Yang, Martin Burtscher, Keshav Pingali and Rajit Manohar

Session 3: Designers using Open-Source Tools (10:45 - 11:05)
Session chair: Rainer Doemer, UCI

10:45 - 10:55: ARL:UT's Experiences in the Free Open-Source VLSI EDA Landscape

Russell Friesenhahn and Johnathan York

11:55 - 11:05: How to Make Open-Source EDA Project Sustainable: a Perspective from Industry
Frank Liu

11:05 - 11:45 Second poster session (all papers)
11:45 - 12:30 Lunch

Session 4: High-Level Tools: Simulation, RTL Synthesis, Verification (12:30 - 02:10)
Session chair: Jose Renau, UCSC

12:30 - 12:40: SystemVerilog Productivity Tools
David Fang

12:40 - 12:50: Invoking and Linking Generators from Multiple Hardware Languages using CoreIR
Ross Daly, Leonard Truong and Pat Hanrahan

12:50 - 01:00: Open-source SoC Workflow in Cloud V
Sherief Reda and Mohamed Shalan

01:00 - 01:10: An Open-Source Python-based Hardware Generation, Simulation, and Verification Framework
Shunning Jiang, Christopher Torng and Christopher Batten

01:10 - 01:20: An Open Source Code Base for Digital Circuit Analysis, Simulation, and Modification
Spencer Millican

01:20 - 01:30: Xyce: Open Source Simulation for Large-Scale Circuits
Jason Verley, Eric Keiter and Heidi Thornquist

01:30 - 01:40: System-on-chip Scheduling Benchmarks for New Technologies
Spencer Millican and Kewal Saluja

01:40 - 01:50: The EPFL Logic Synthesis Libraries
Mathias Soeken, Heinz Riener, Winston Haaswijk, Eleonora Testa and Giovanni De Micheli

01:50 - 02:00: Hierarchical Asynchronous Circuit Kompiler Toolkit
David Fang

02:00 - 02:10: RISC: Recoding Infrastructure for SystemC, Open Source Framework for Parallel Simulation
Rainer Doemer, Zhongqi Cheng, Daniel Mendoza and Ajit Dingankar

2:10 - 2:40 Third Poster Session (all papers)

Session 5: Planned & Educational Tools (02:40 - 03:10)
Session chair: Jose Luis A Guntzel, Federal University of Santa Catarina

02:40 - 02:50: An EDA Tool for Co-designing High-Performance Processors and Emerging Cooling Technologies
Zihao Yuan, Geoffrey Vaartstra, Prachi Shukla, Mostafa Said, Sherief Reda, Evelyn Wang and Ayse Kivilcim Coskun

02:50 - 03:00: METRICS 2.0: A Machine-Learning Based Optimization System for IC Design
Soheil Hashemi, Andrew Kahng, Sherief Reda and Mingyu Woo

03:00 - 03:10: TESTCAD: A Verified Education Toolset for a Course in Digital Testing
Spencer Millican and Kewal Saluja

Session 6: Physical Design Tools (03:10 - 04:00)
Session chair: Rajit Manohar, Yale University

03:10 - 03:20: OpenTimer 2.0: A High-performance Timing Analysis Tool for VLSI Systems
Tsung-Wei Huang, Chun-Xun Lin and Martin Wong

03:20 - 03:30: Low-Power Design with Open-Source Hardware: Opportunities and Challenges
Vaibhav Verma, Xinfei Guo and Mircea Stan

03:30 - 03:40: Ophidian: an Open-Source Library for Physical Design Research and Teaching
Renan Netto, Tiago Augusto Fontana, Sheiny Fabre, Bernardo Ferrari, Vinicius Livramento, Thiago Barbato, João Souto, Chrystian Guth, Laércio Pilla and José Luís Güntzel

03:40 - 03:50: OpenMPL: An Open Source Layout Decomposer
Qi Sun, Yibo Lin, Iris Hui-Ru Jiang, Bei Yu and David Z. Pan

03:50 - 04:00: Hammer: Enabling Reusable Physical Design
Edward Wang, Adam Izraelevitz, Colin Schmidt, Borivoje Nikolić, Elad Alon and Jonathan Bachrach

4:00 - 4:30 Fourth poster Session (all papers)
Afternoon Coffee Break with snacks

4:30 - 5:00 Panel: Where are we and where to head next?
Moderator: Andrew B. Kahng
Panelists: Andreas Olofsson, Leon Stok, Tim Edwards and Jose Renau

5:00 announcement of best tool based on votes

Additional posters:

Industrial ASIC Design using Open Source EDA Flow
M. Kasem and T. Edwards.

An Almost-There, Open-Source Netlist Through Detailed Routing Tool Chain for FinFET Nodes
Bangqi Xu, Andrew B. Kahng, Mingyu Woo, Uday Mallappa, Minsoo Kim, Mateus Fogaça and Ricardo Reis